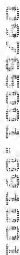
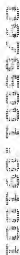
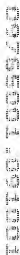
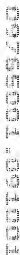
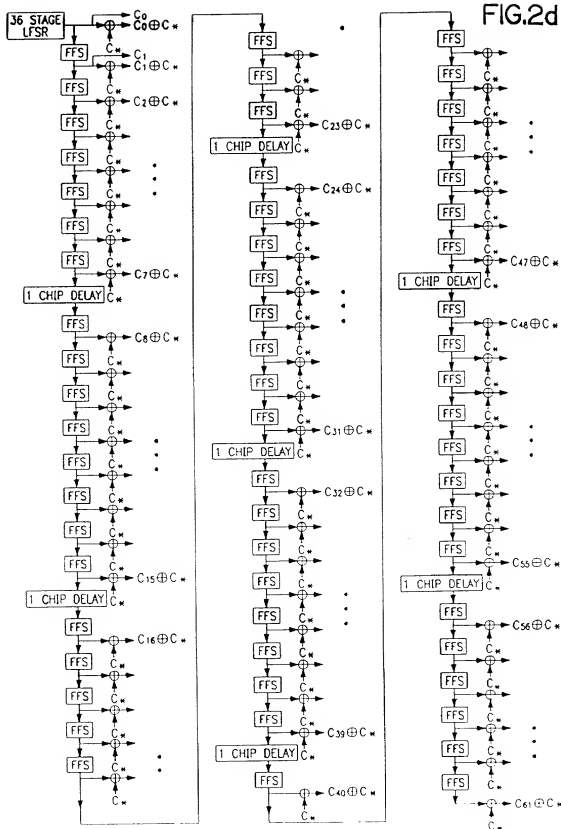


[illegible][illegible]

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[illegible]



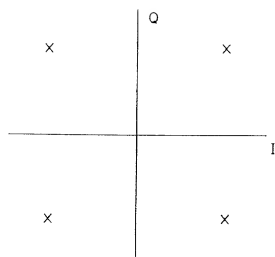


FIG. 3a

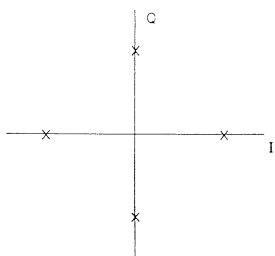


FIG. 3b

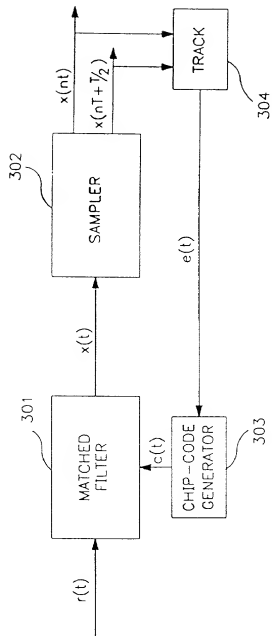
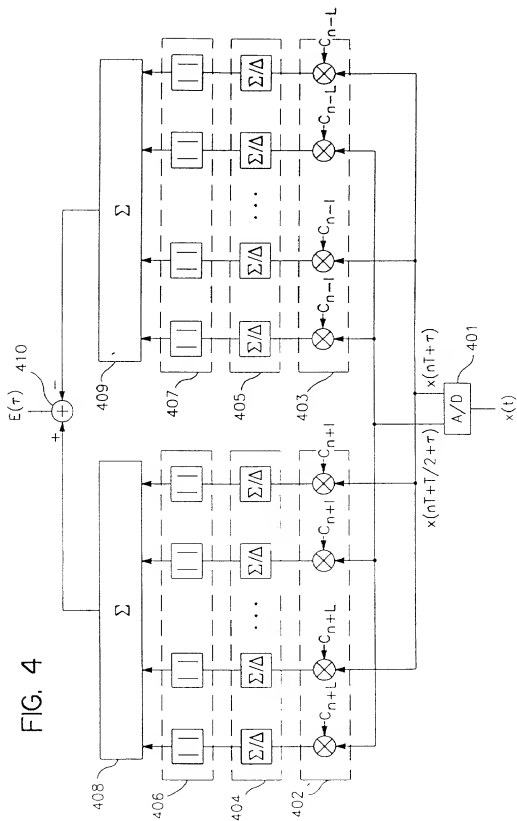


FIG. 3c



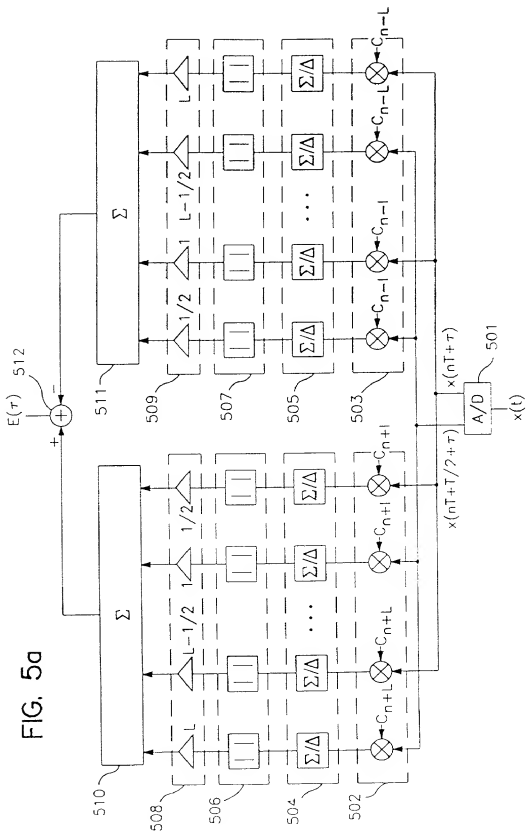
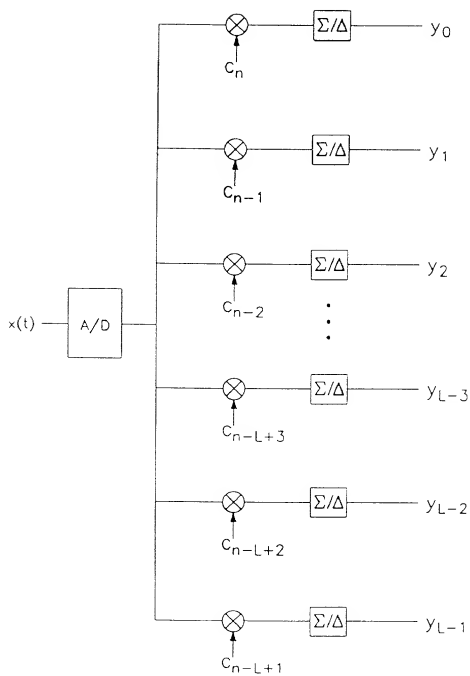


FIG. 5b



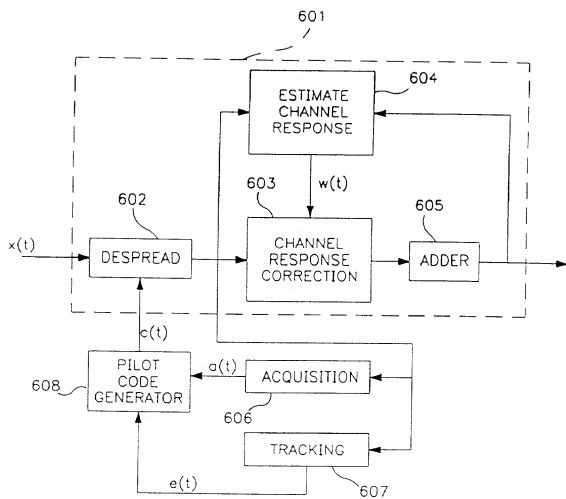


FIG. 6



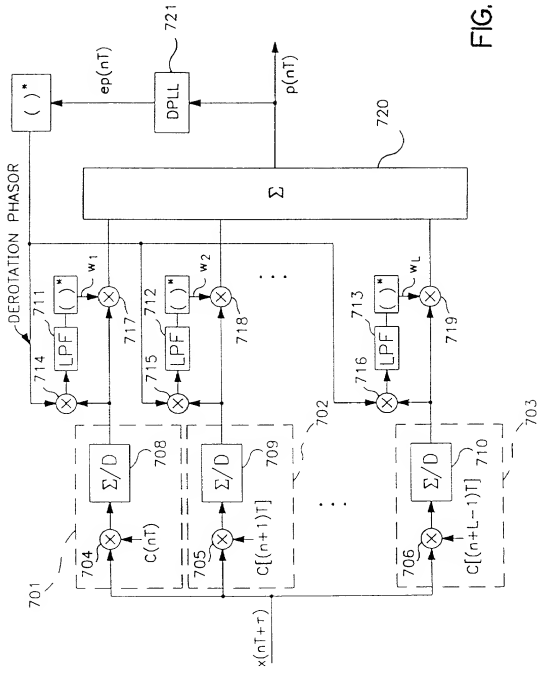


FIG. 7

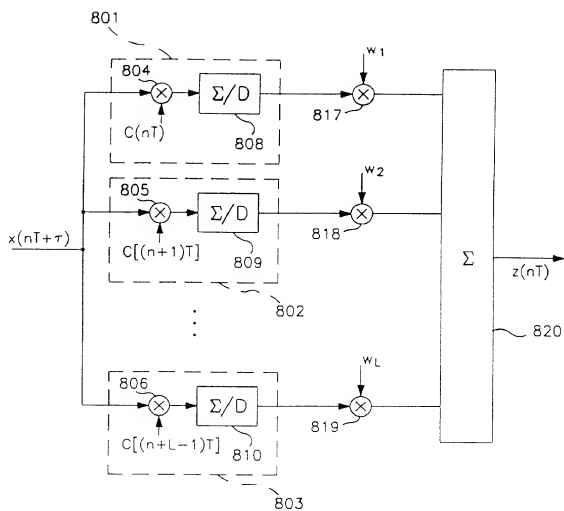


FIG. 8a

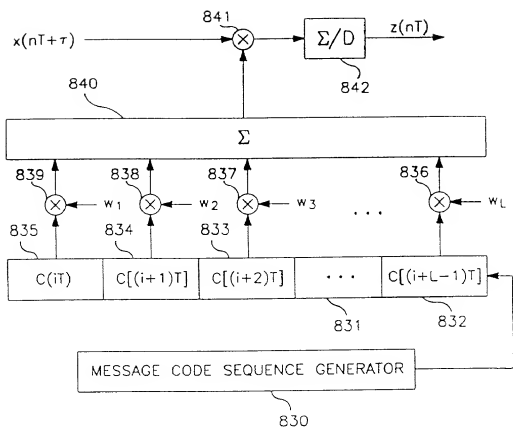


FIG. 8b

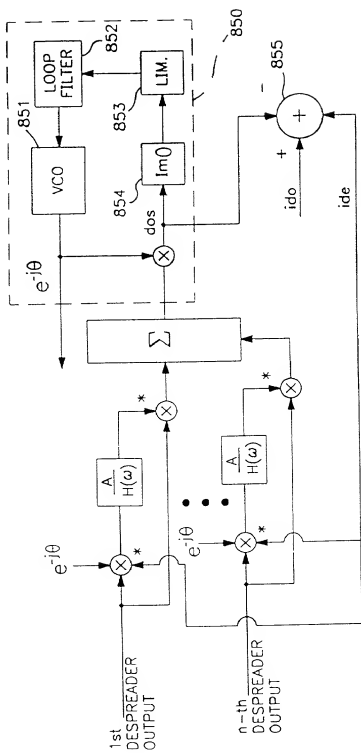


FIG. 8c

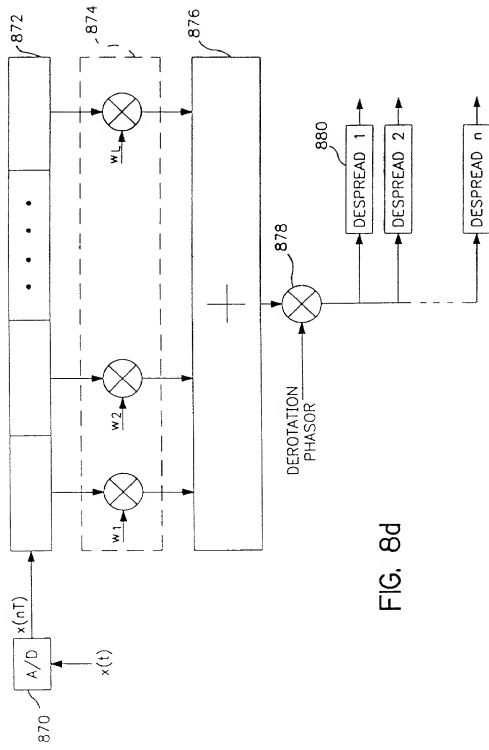


FIG. 8d

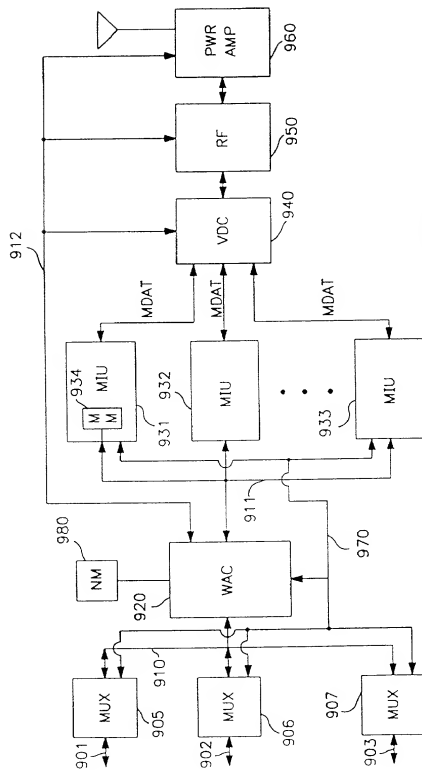


FIG. 9

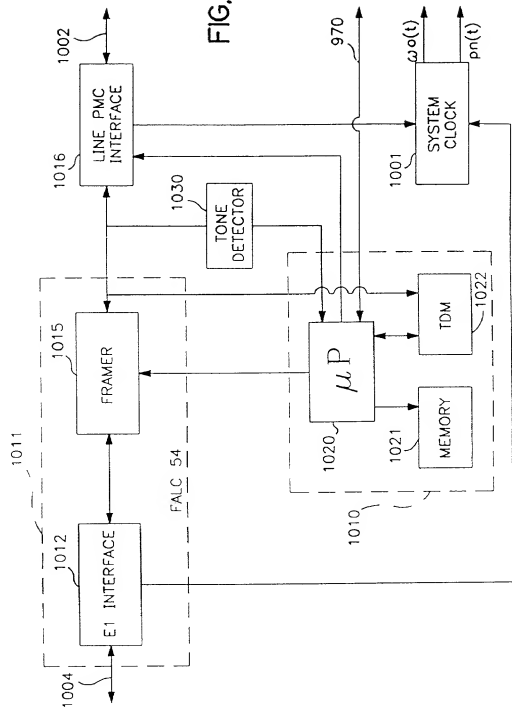


FIG. 10

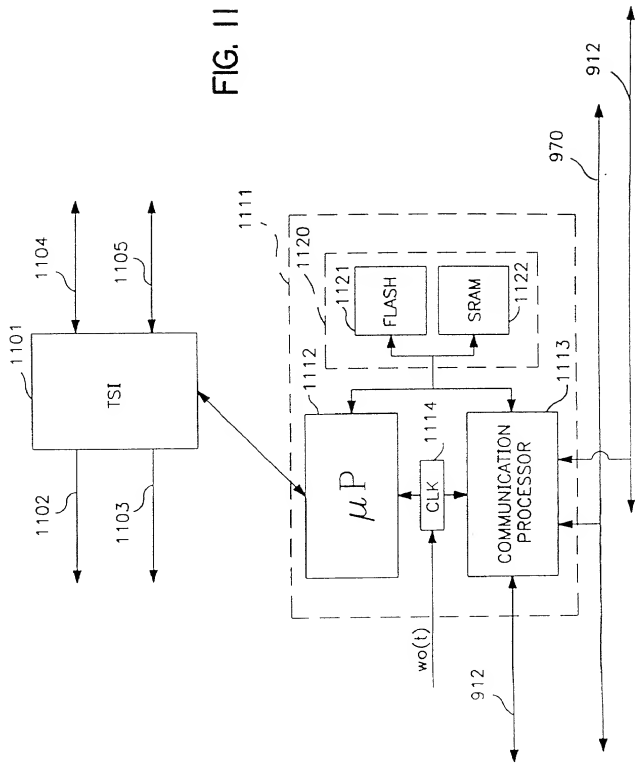


FIG. 11



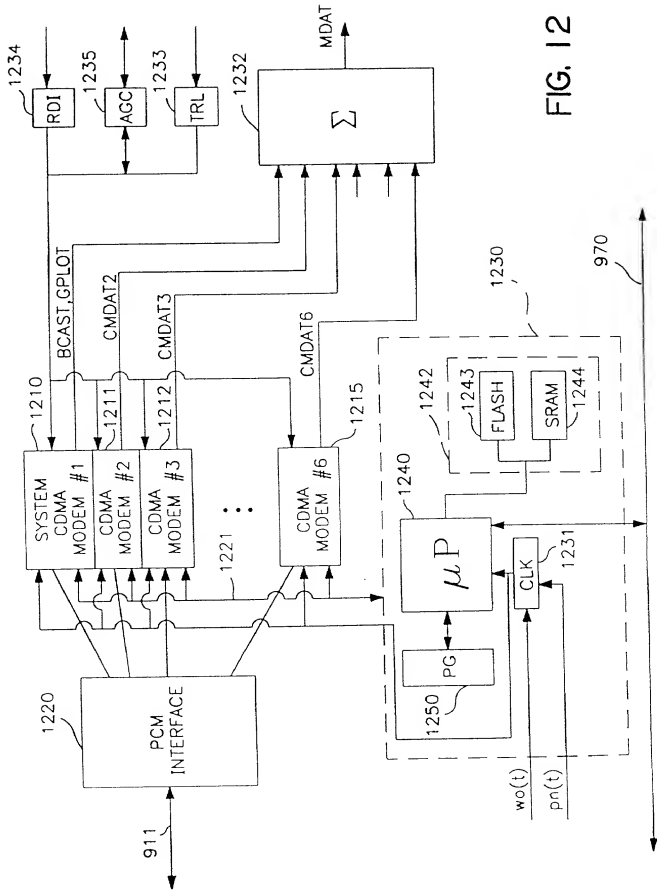


FIG. 12

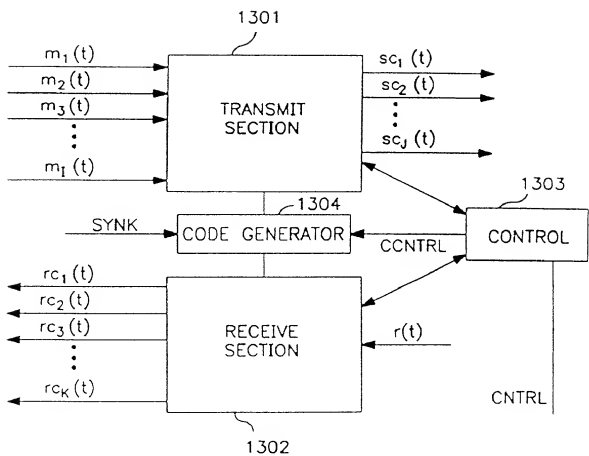


FIG. 13

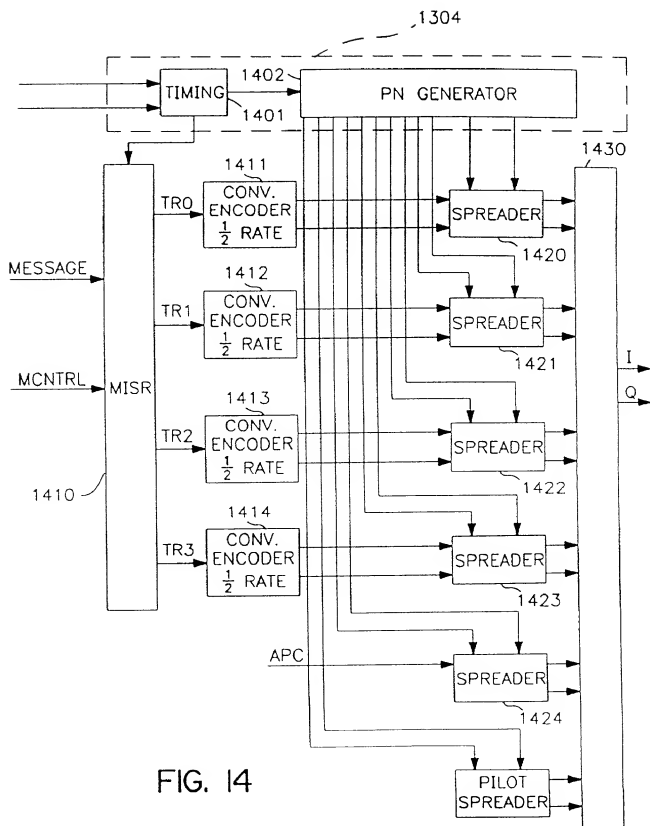
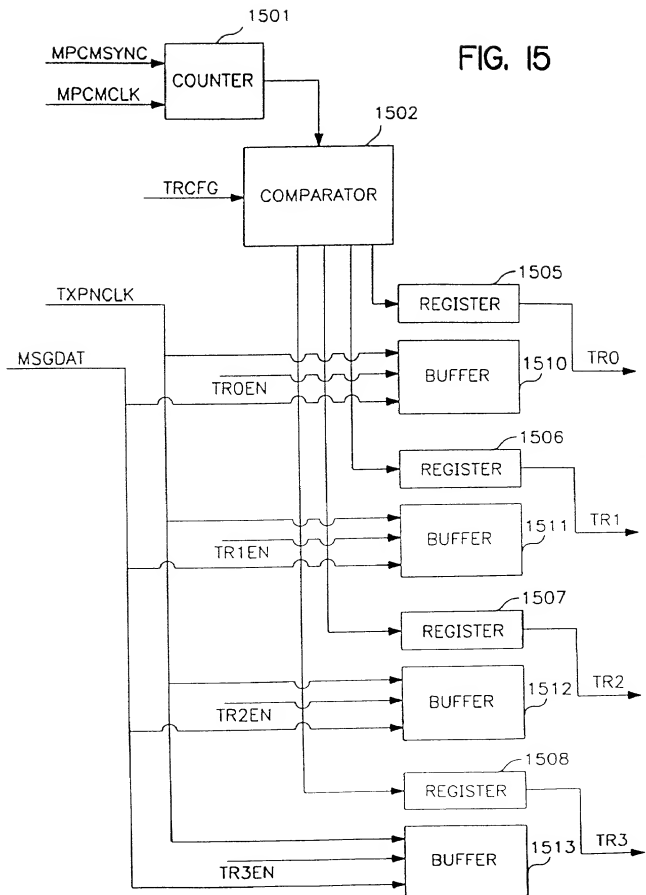


FIG. 14

FIG. 15



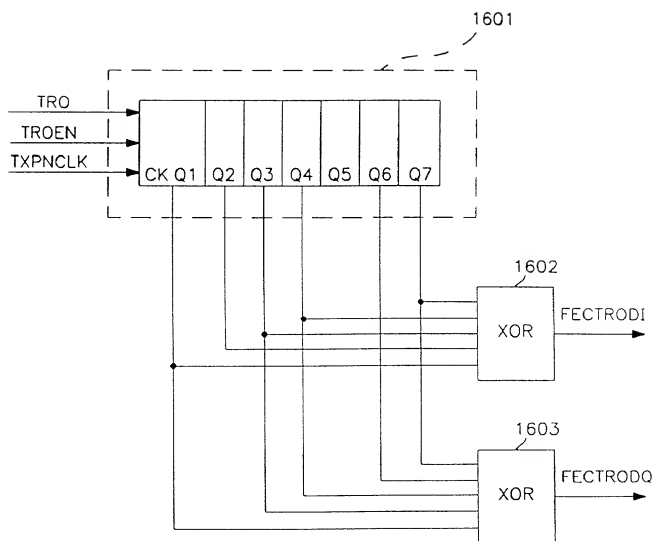


FIG. 16

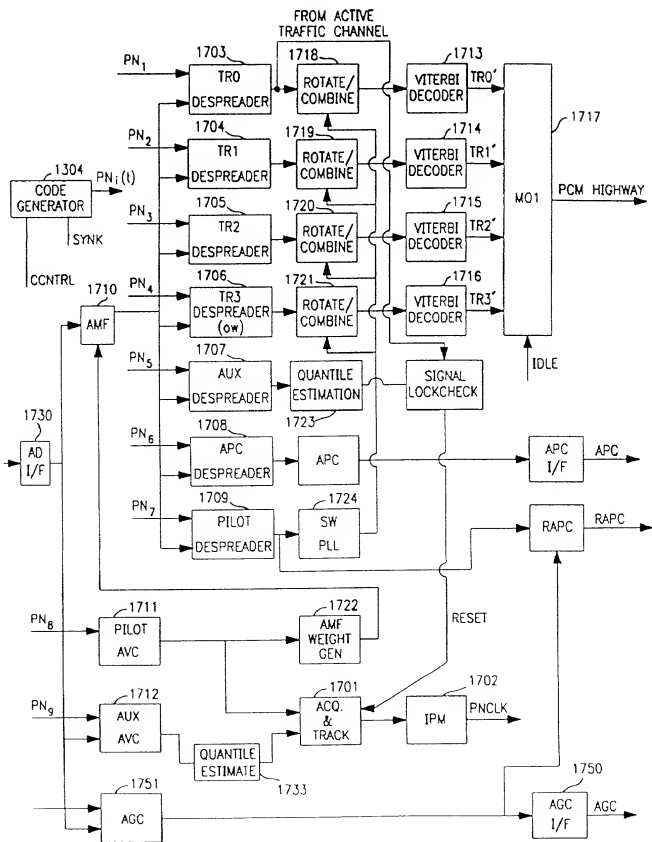


FIG. 17

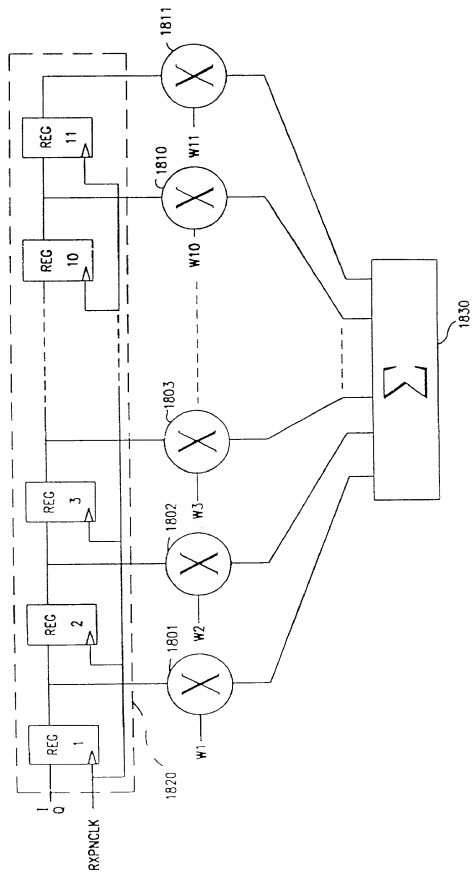


FIG. 18

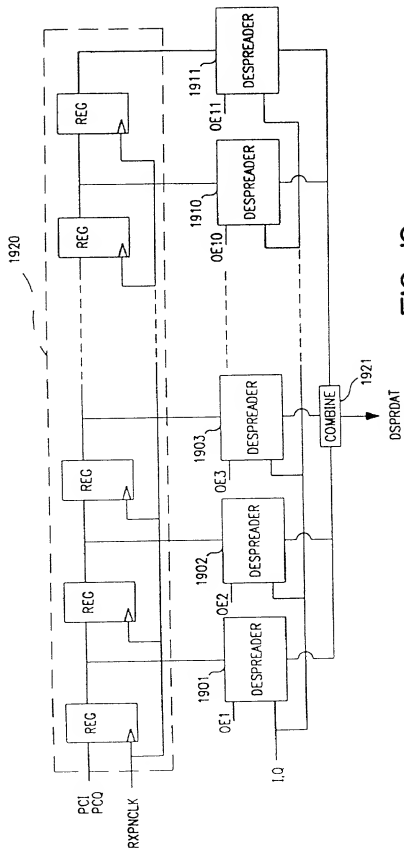


FIG. 19



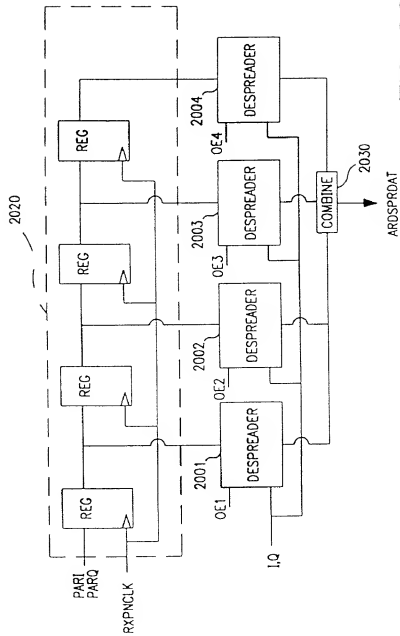


FIG. 20

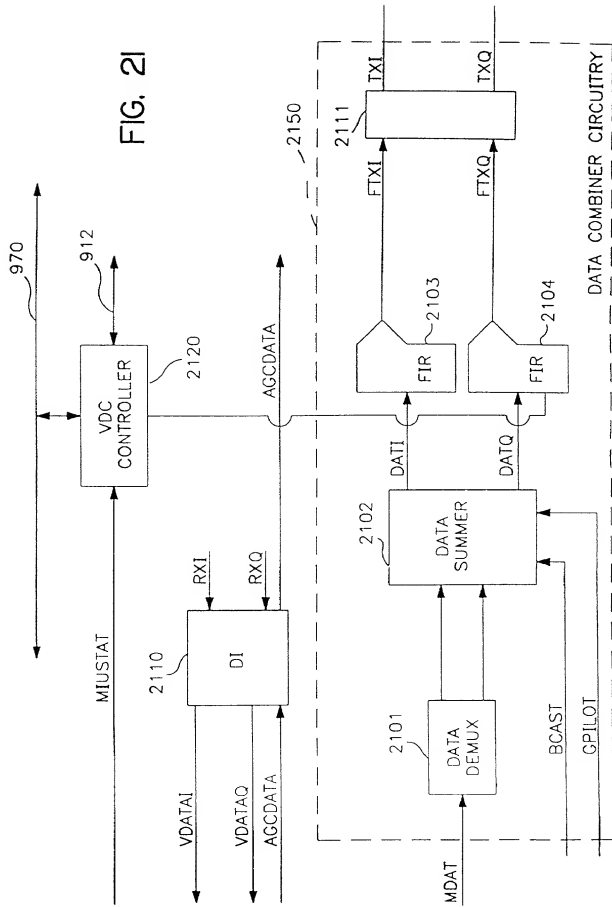


FIG. 21

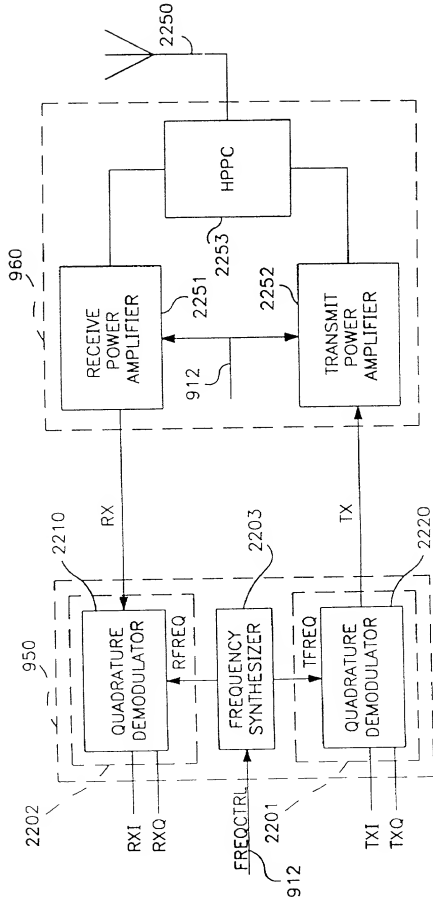


FIG. 22

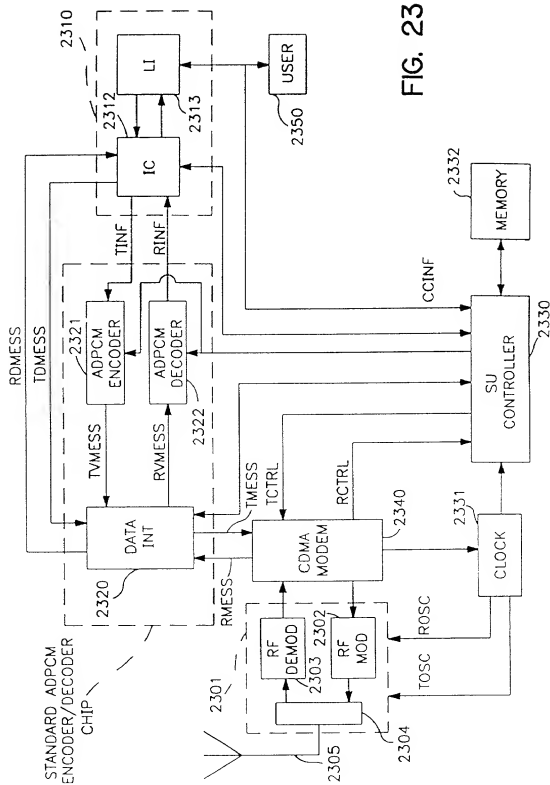


FIG. 23

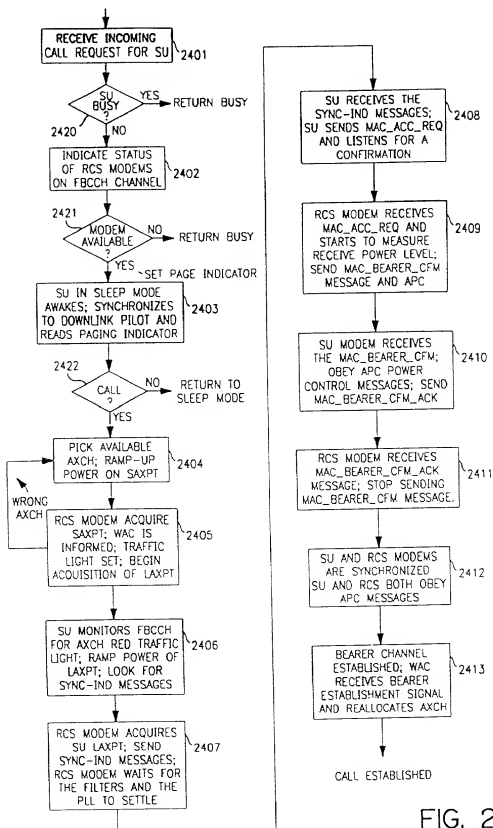


FIG. 24

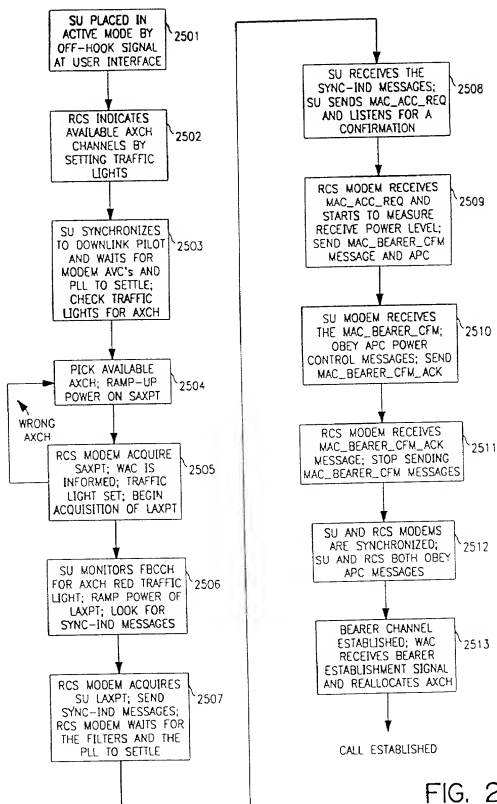


FIG. 25

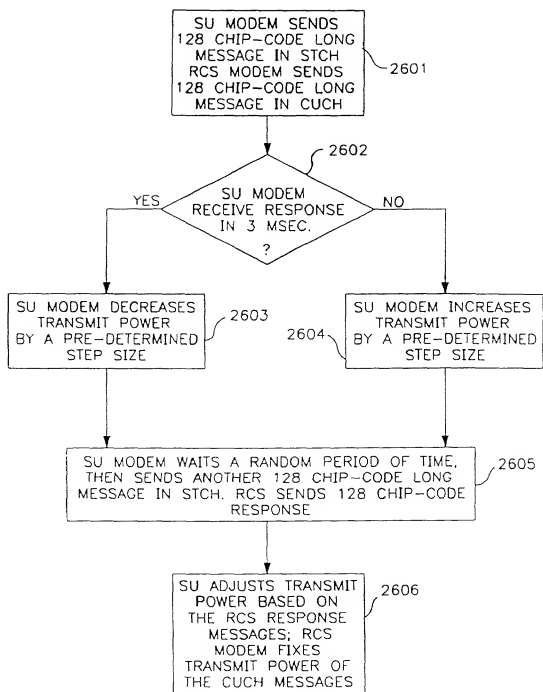


FIG. 26

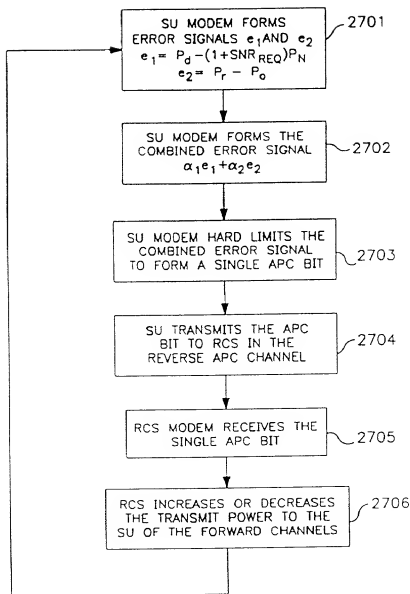


FIG. 27



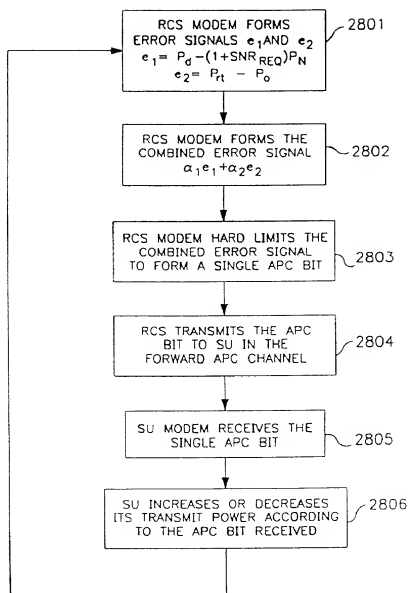


FIG. 28

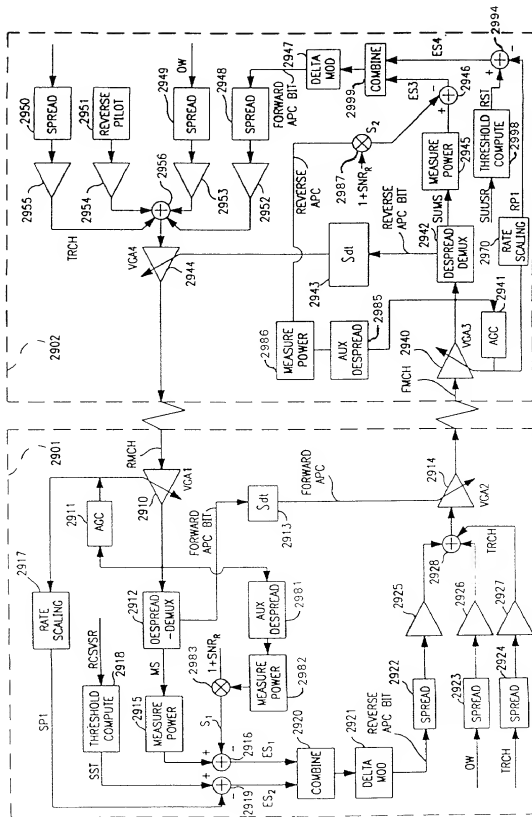


FIG. 20



FIG. 31

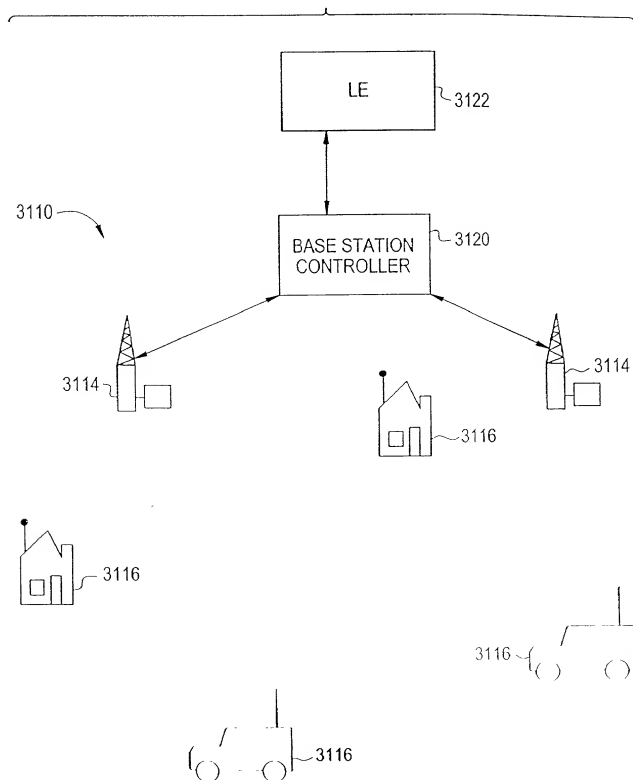


FIG. 32

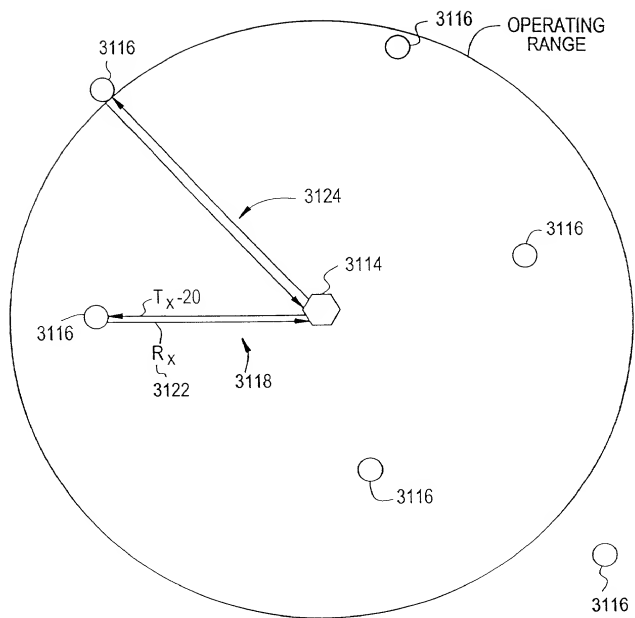
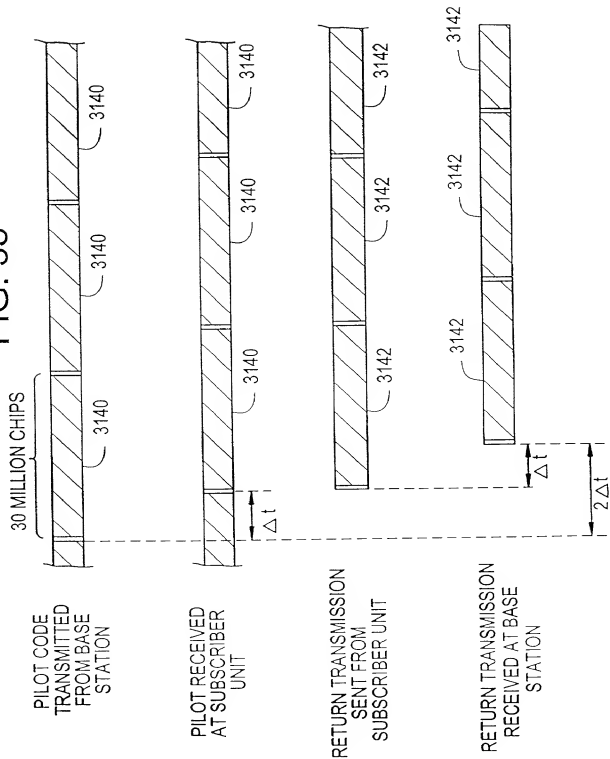


FIG. 33



# FIG. 34

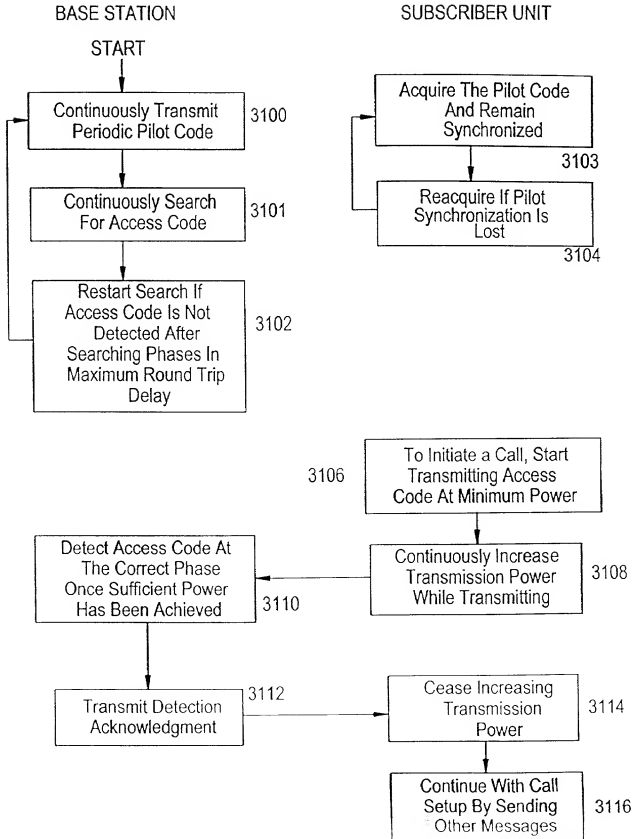


FIG. 35

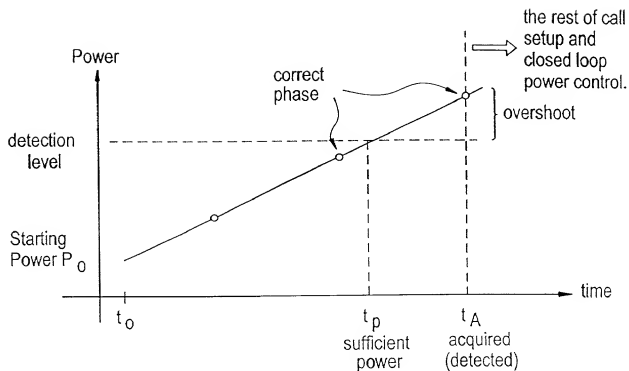
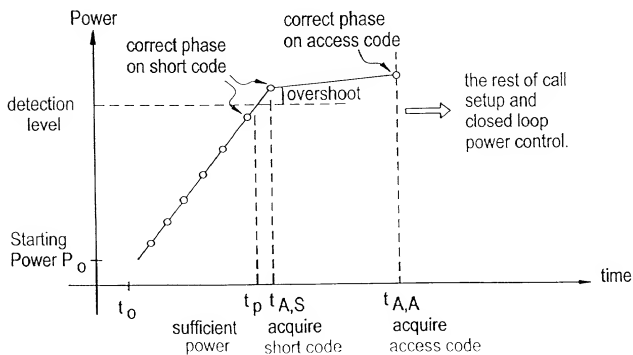


FIG. 37





# FIG. 36A

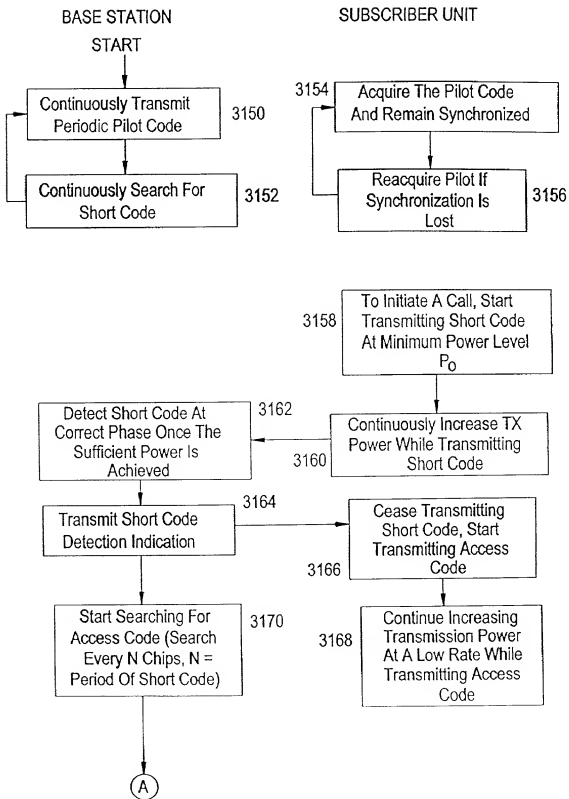


FIG. 36B

BASE STATION

SUBSCRIBER UNIT

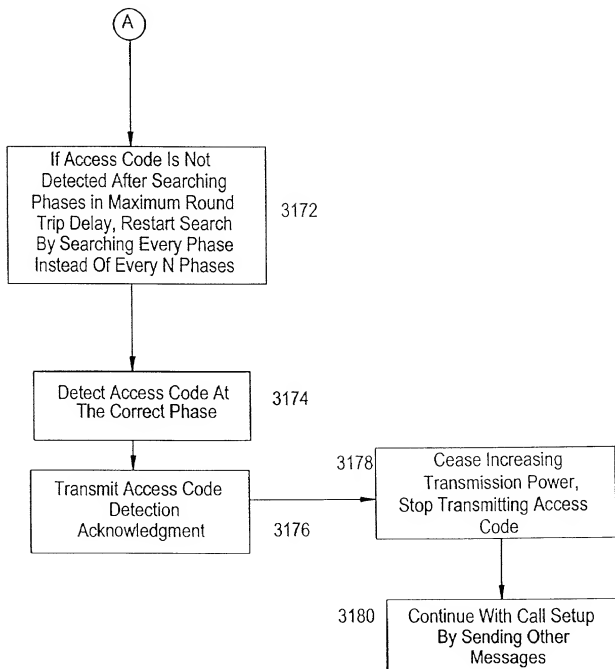


FIG. 38

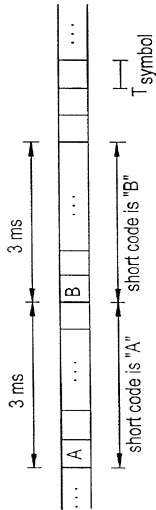


FIG. 39

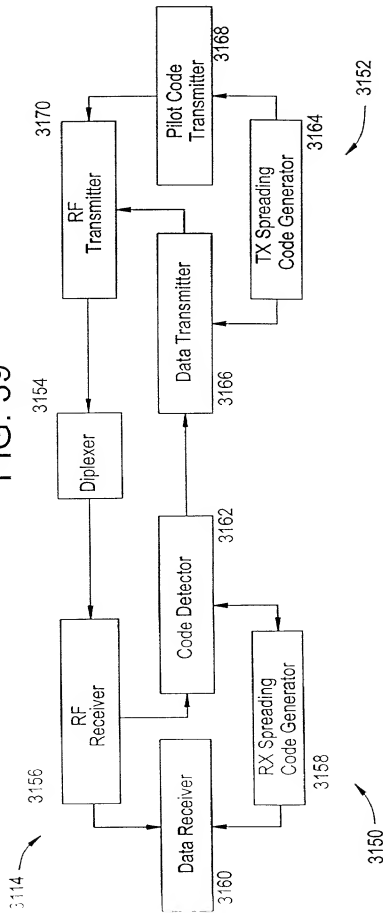


FIG. 40

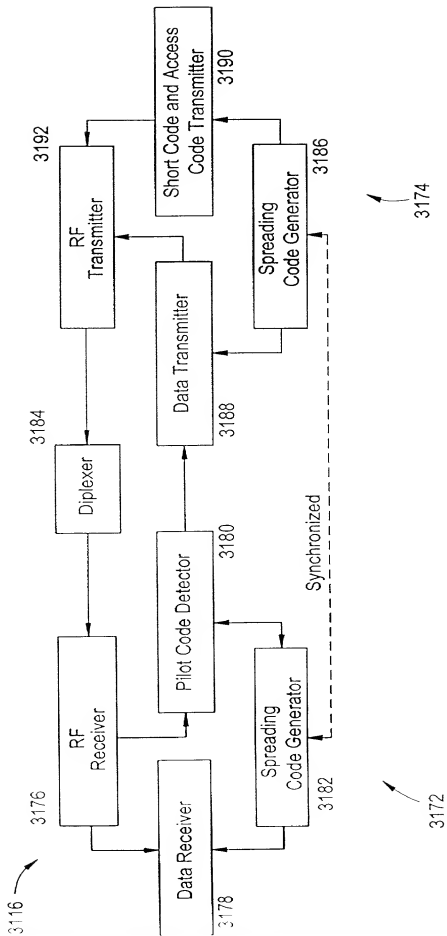


FIG. 41A

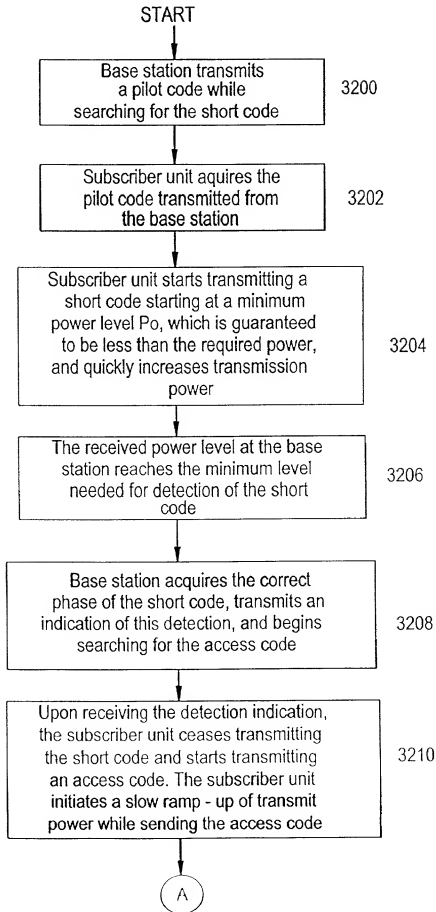


FIG. 41B

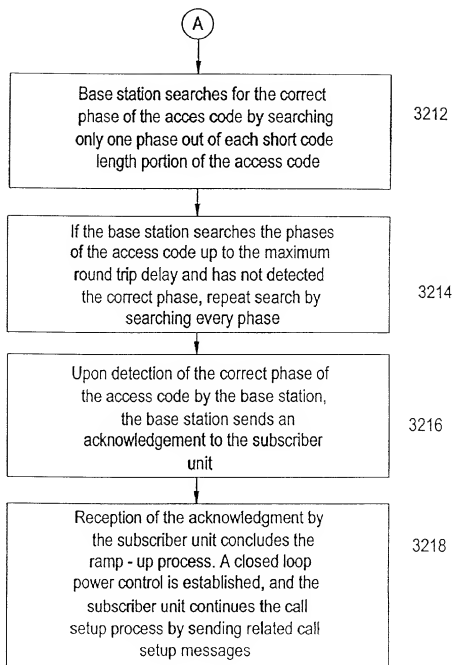


FIG. 42  
PRIOR ART

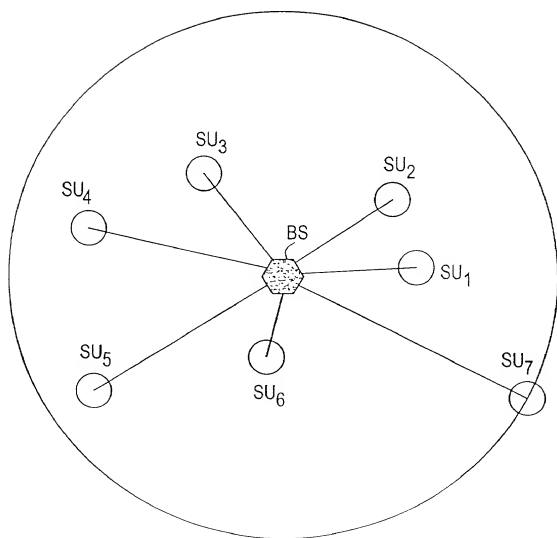


FIG. 43  
(PRIOR ART)

Mean Cell Sweep Time, FSU @ 20 KM

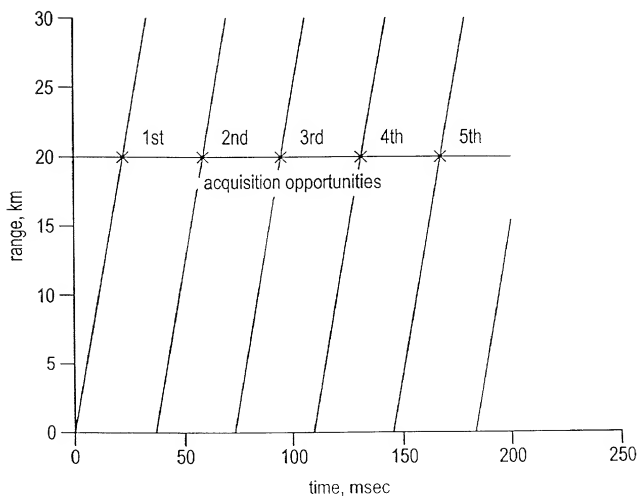
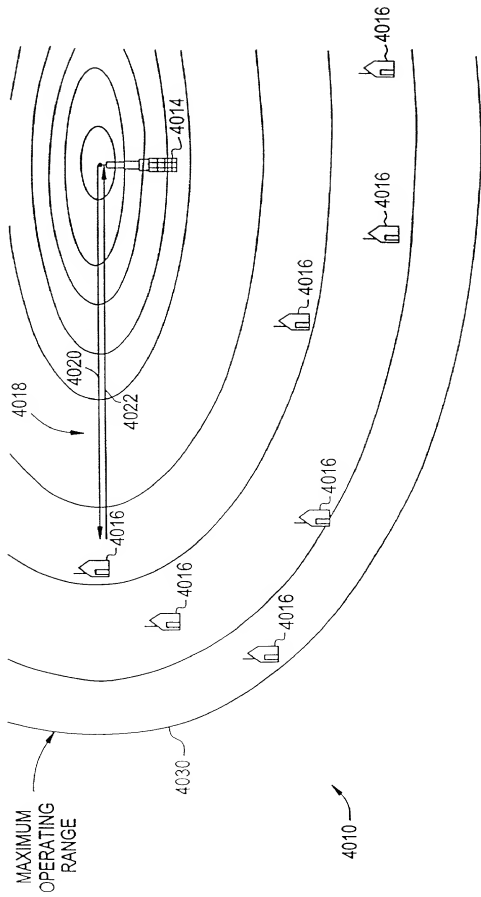




FIG. 44



# FIG. 45

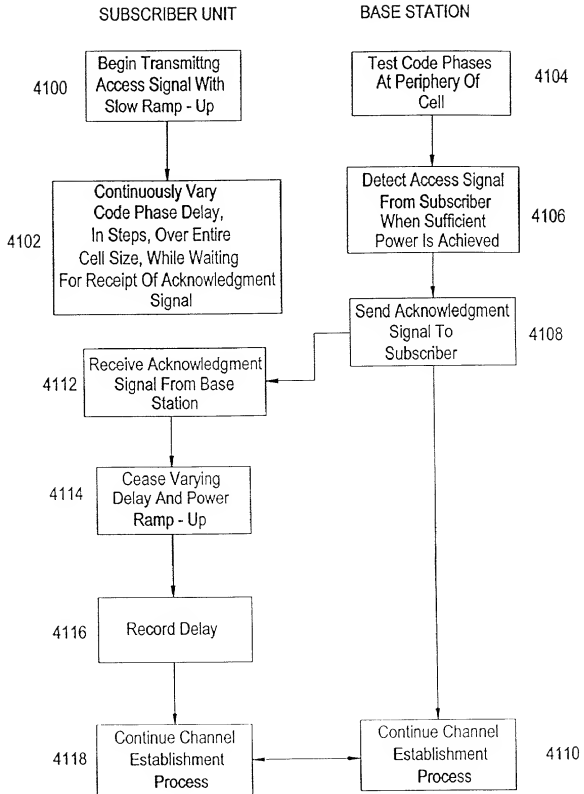


FIG. 46

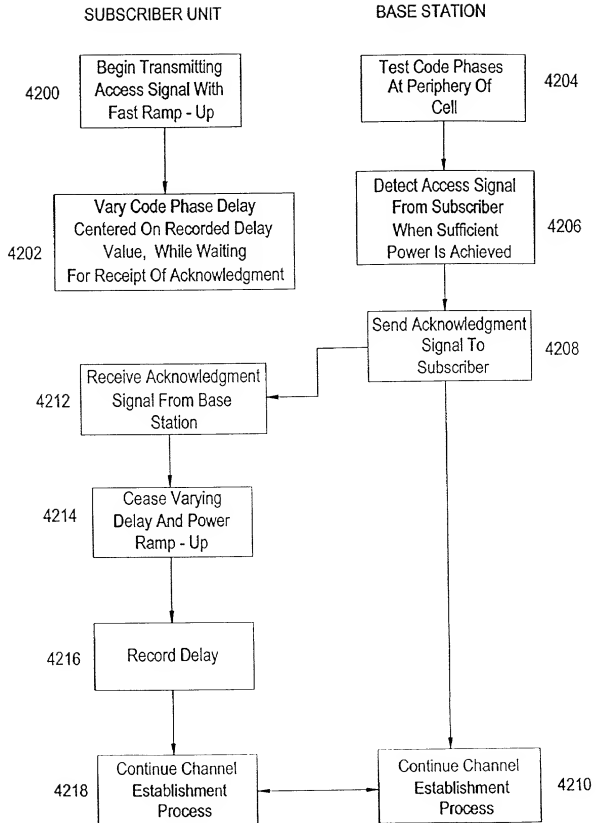


FIG. 47

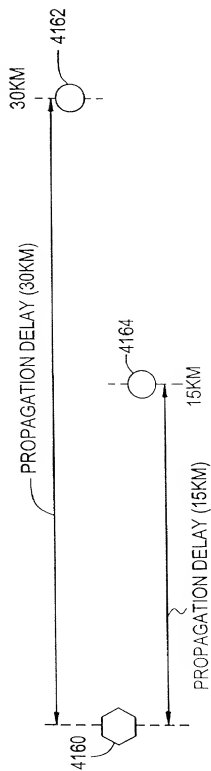


FIG. 48

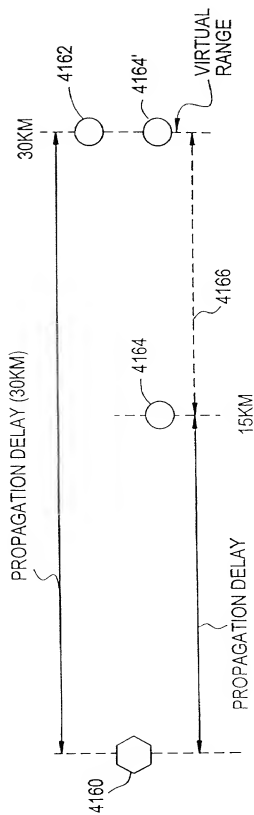


FIG. 49

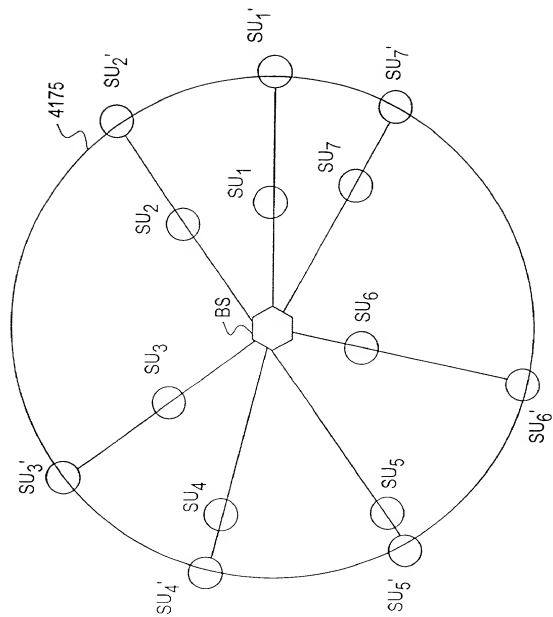
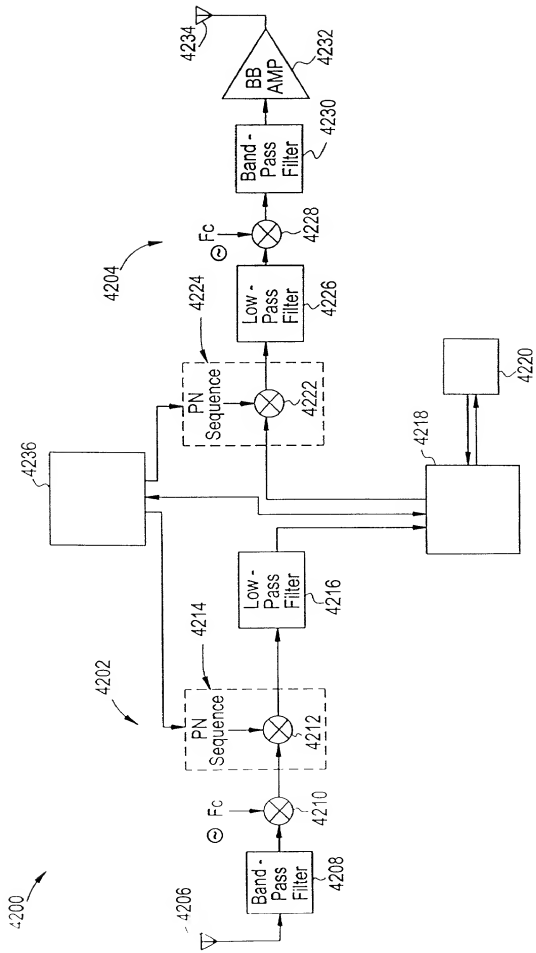


FIG. 50



# FIG. 51

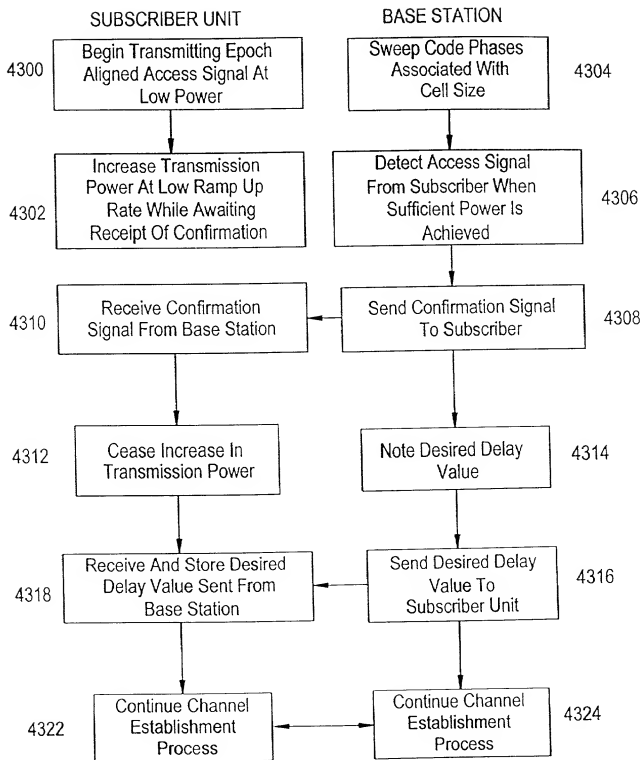
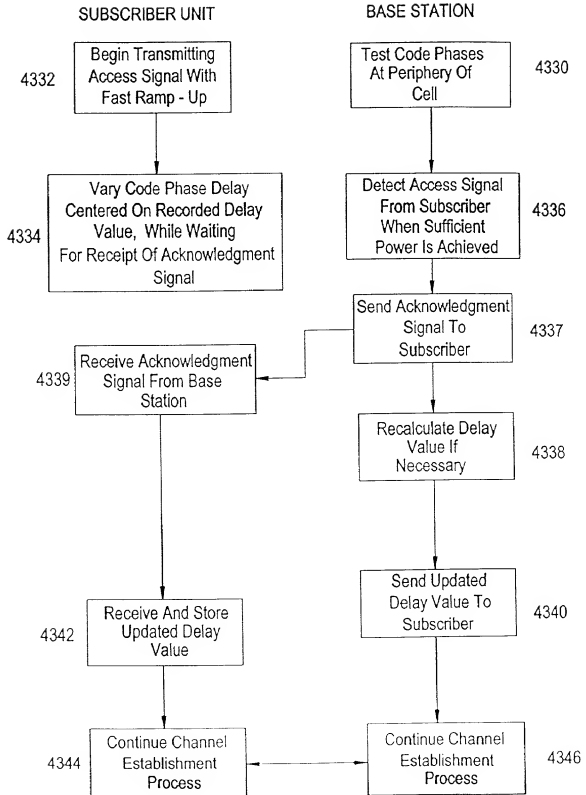


FIG. 52





# FIG. 53

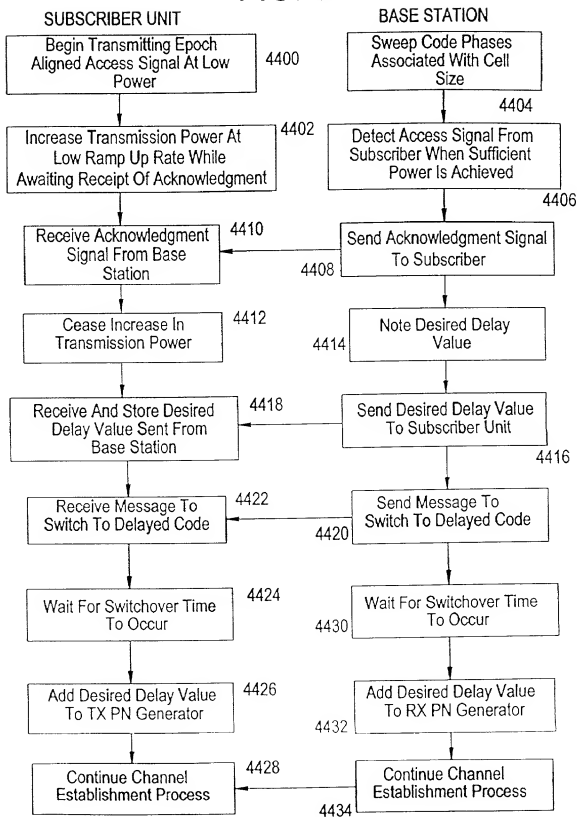


FIG. 54  
PRIOR ART

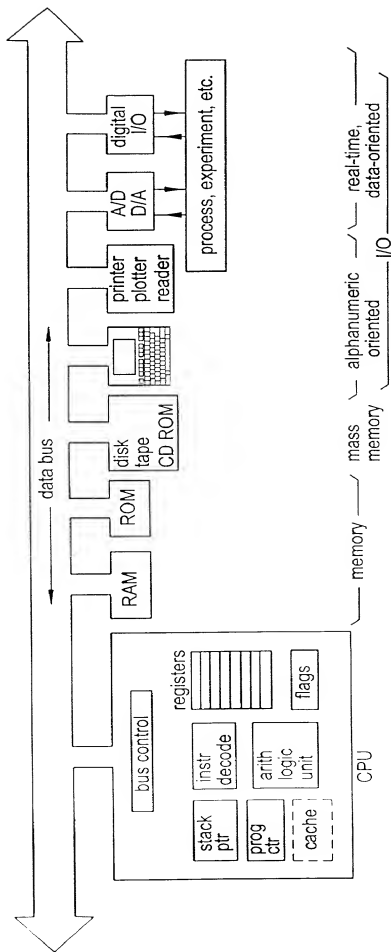


FIG. 55  
PRIOR ART

BUS	RAW bandwidth (Mbyte/s)	Data width	Address width	Block xfer?	MUXed data/adr?	Multimaster?	Sync/Async	IRQ Lines a	Drivers	Connector b	Comments
STD bus		8	16	—	—	—	S	1	TTL	CE	controller-type applications
PC XT	1.2	8	20	—	—	—	S	5E	TTL	CE	original IBM PC & compatibles
PC AT	5.3	8,16	20,24	—	—	(c)	S	10E	TTL	CE	accepts PC/XT cards
EISA	33	8,16,32	20,24,32	•	—	•	S	11P	TTL	CE	enhanced PC/AT; auto-configure
MicroChannel	20	8,16,(32)	24,(32)	•	—	•	A	11	TTL	CE	IBM PS/2; auto-configure
Q-bus	2	16	22	—	—	•	A	4	(d)	CE	LSI-11, $\mu$ VAX-II; daisy-chained IACK
Multibus I	10	8,16	20,24	—	—	•	A	4	TTL	CE	Intel; SUN-I and others
CAMAC	3	24	9	—	—	—	S	L	TTL/OC	CE	data acquisition & control bus
VAX BI	13.3	8,16,24,32	32	•	•	•	S	4	TTL	ZIF	VAX 780, 8600 series; parity
Multibus II	40	8,16,24,32	16,32	•	•	•	S	M	TTL	DIN	parity; 40MB/s for blk xfer, 20M otherwise
NuBus	40	32	32	•	•	•	S	M	TTL	DIN	Macintosh II adds 1 dedicated INT per slot; ""
VME	40	8,16,32	16,24,32	•	—	•	A	7	TTL	DIN	daisy-chained IACK; SUN-3
Futurebus	120					•	A	—	(d)	H	communication across many crates
Fastbus	160	32	32	•	•	•	A	M	ECL	H	

(a) E-edge-sensitive; L-LAM ("look at me"); M-"int" via bus mastership;

P-programmable edge-or level-sensitive interrupts.

(b) CE-card-edge; DIN-2-part "Eurocard" 96-pin connector.

H-high density 2-part conn. (c) almost. (d) National Semi special.

FIG. 56

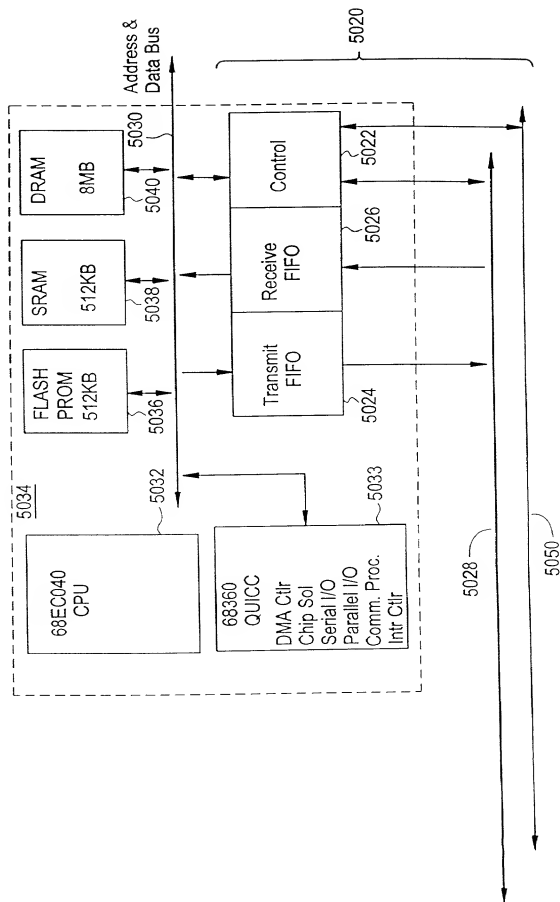


FIG. 57A

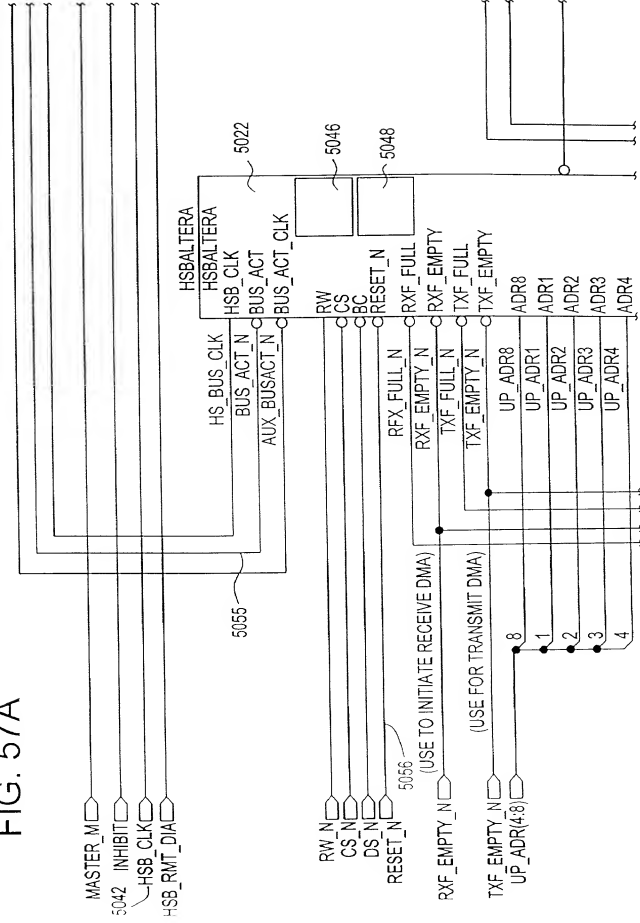
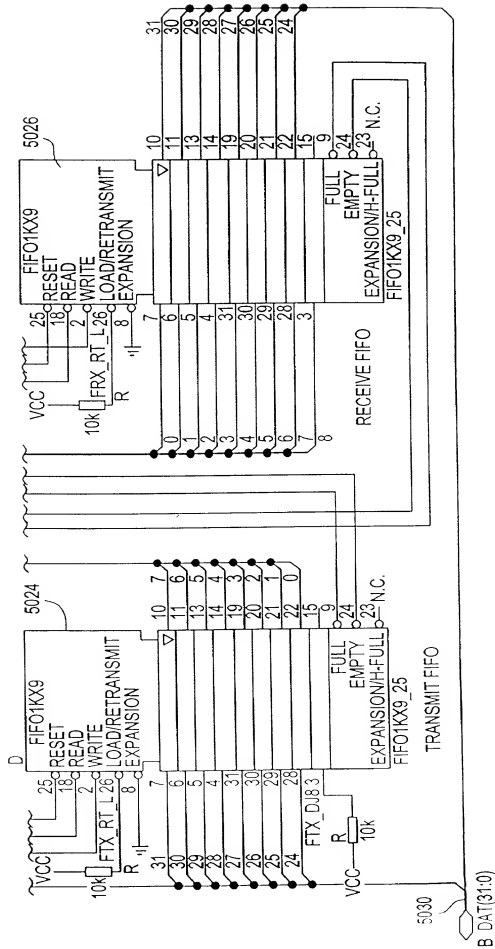


FIG. 57B

FIG. 57B is a detailed schematic diagram of the RX and TX FIFOs. The diagram shows the internal logic of the RX\_FIFO\_READ and TX\_FIFO\_READ blocks, including the RX(8:0) and TX(7:8) data buses, and the RX\_FIFO\_READ and TX\_FIFO\_READ control signals. The RX\_FIFO\_READ block is connected to the RX(8:0) data bus and the RX\_FIFO\_READ control signal. The TX\_FIFO\_READ block is connected to the TX(7:8) data bus and the TX\_FIFO\_READ control signal. The RX\_FIFO\_READ block is also connected to the RX\_FIFO\_READ control signal. The TX\_FIFO\_READ block is also connected to the TX\_FIFO\_READ control signal. The RX\_FIFO\_READ block is also connected to the RX\_FIFO\_READ control signal. The TX\_FIFO\_READ block is also connected to the TX\_FIFO\_READ control signal.

FIG. 57C



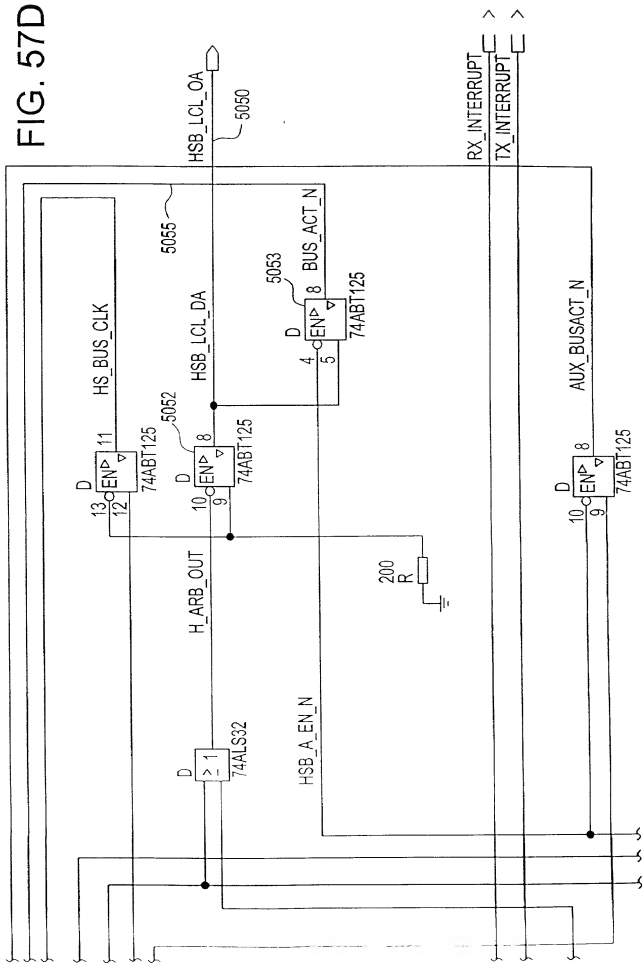




FIG. 57E

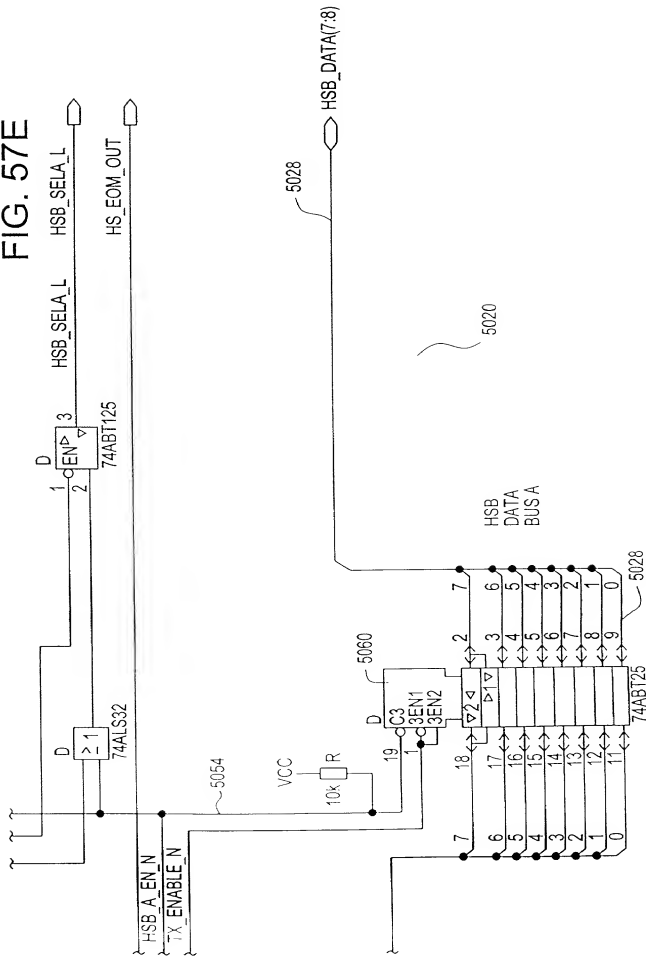


FIG. 58

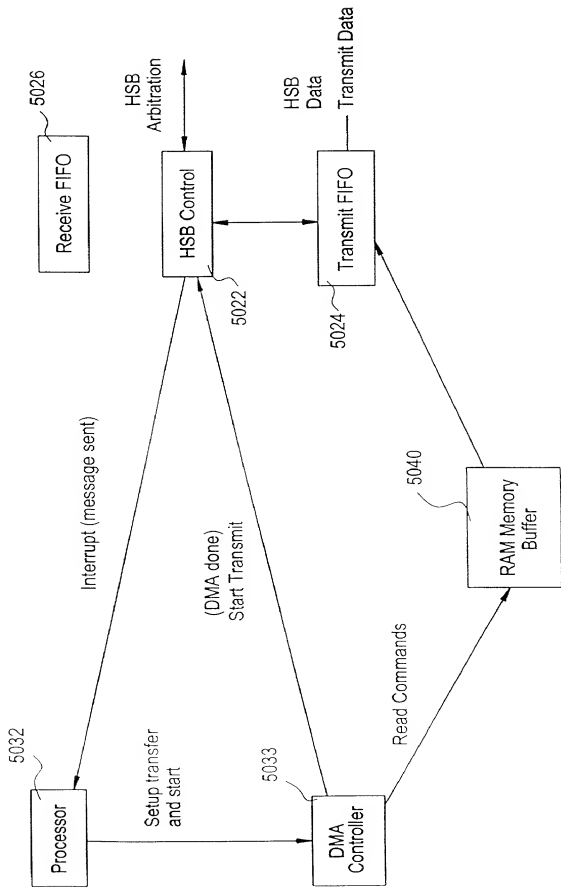


FIG. 59

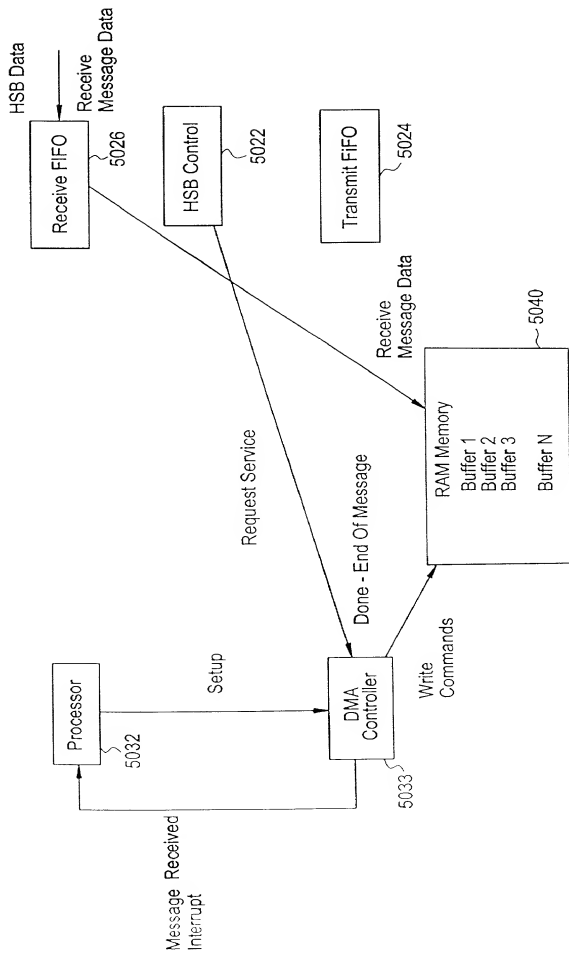


FIG. 60

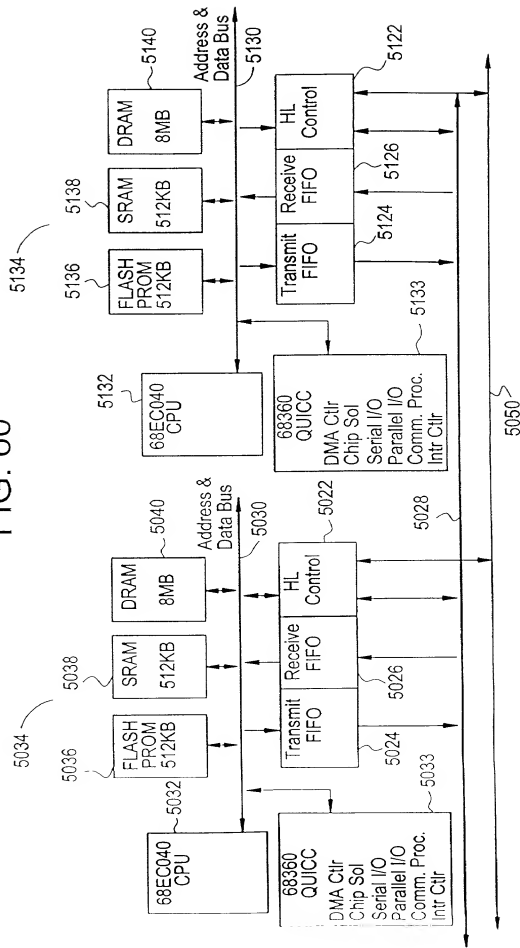


FIG. 61

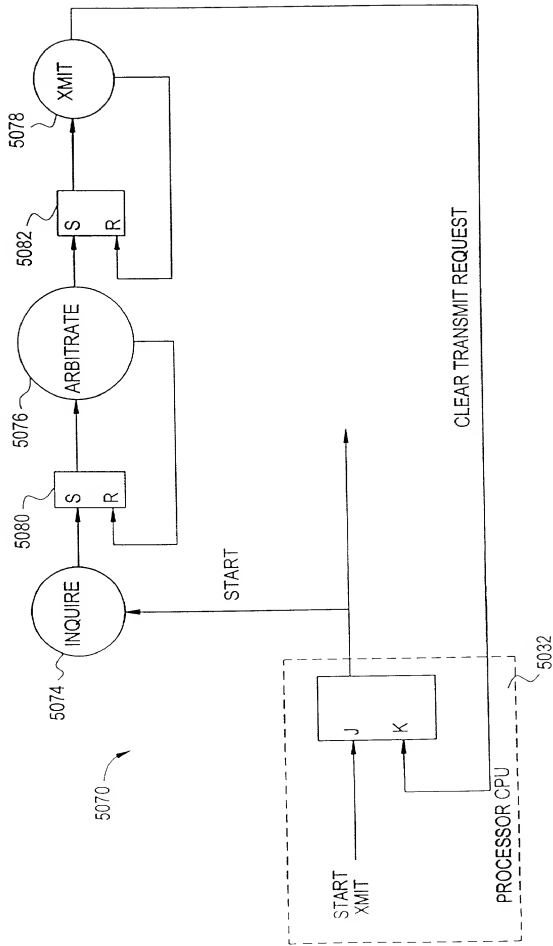


FIG. 62

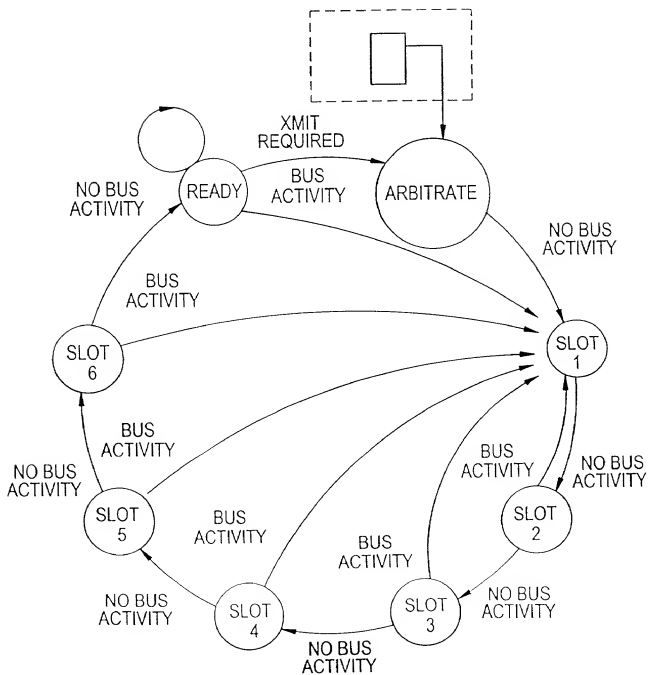


FIG. 63

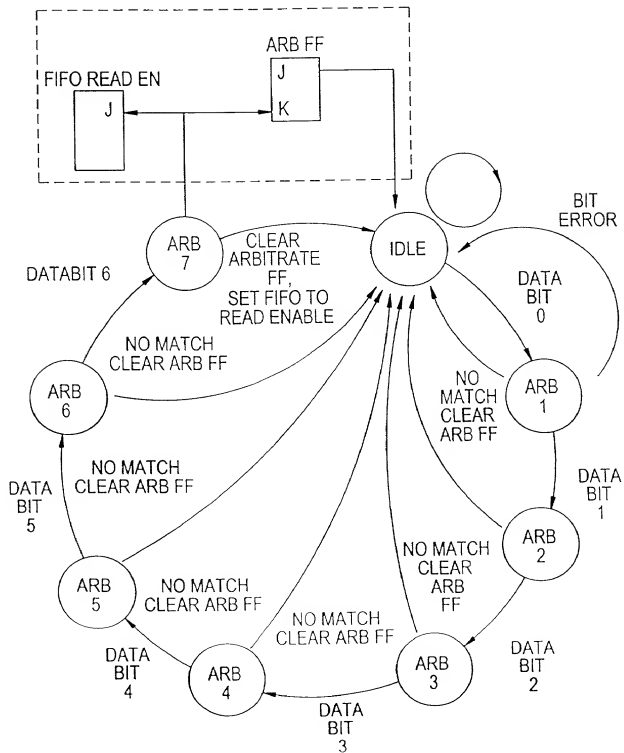


FIG. 64

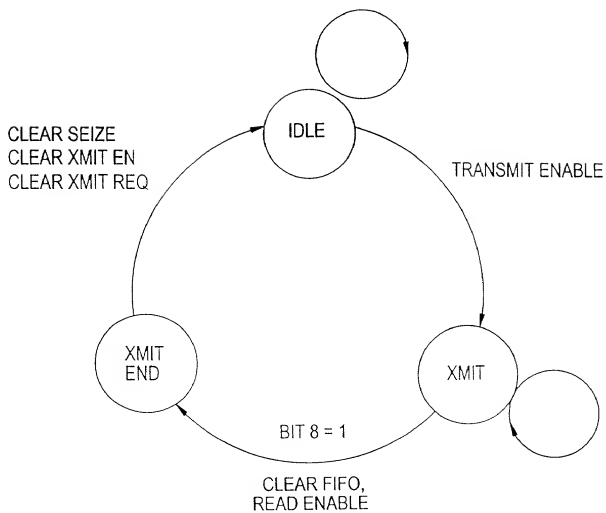


FIG. 65

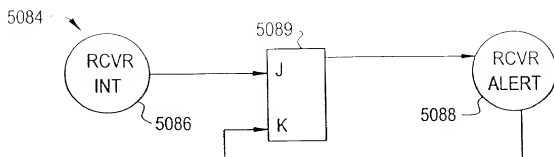




FIG. 66

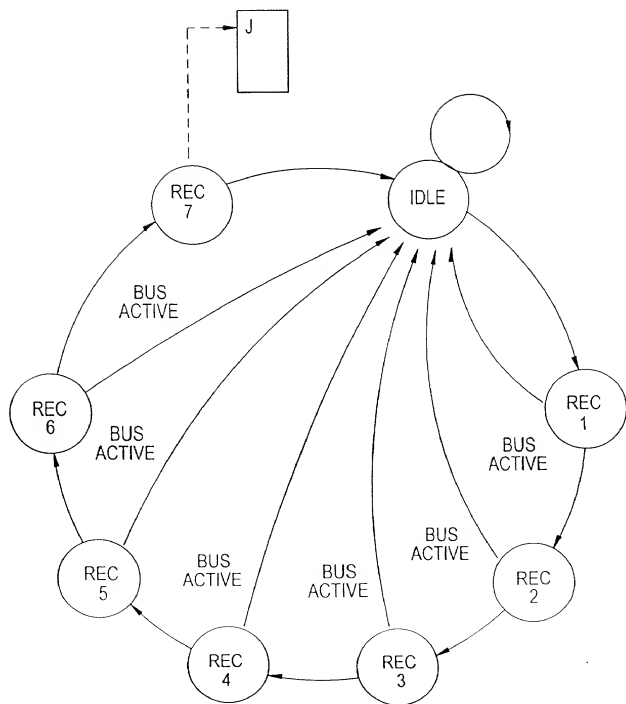


FIG. 67

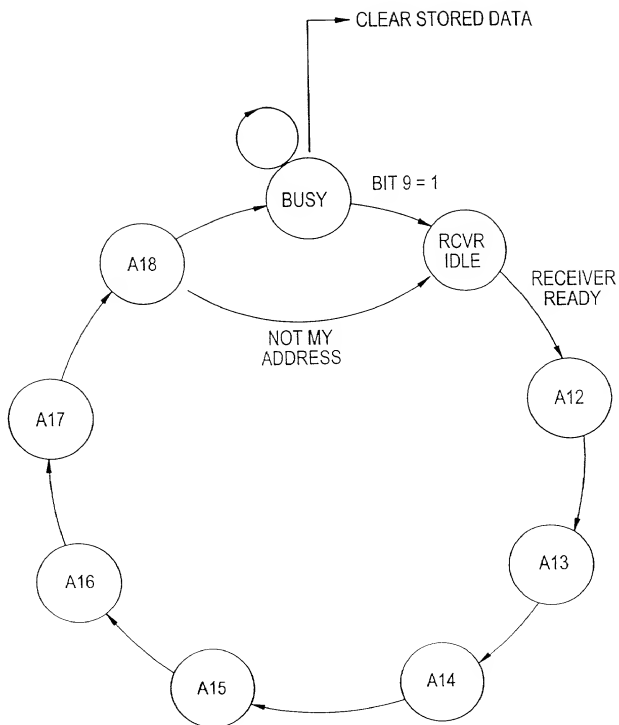


FIG. 68

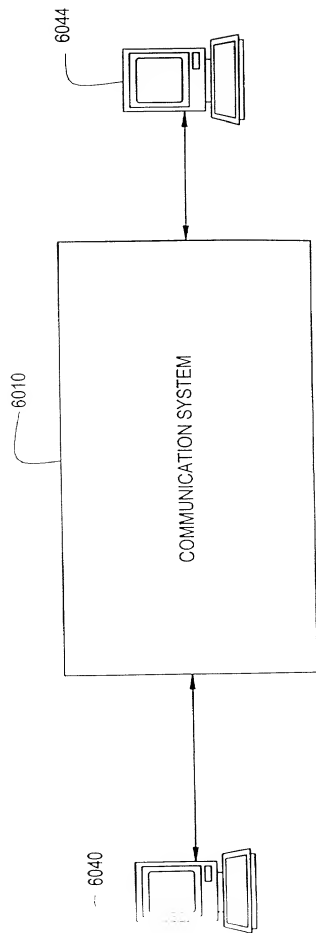


FIG. 69  
PRIOR ART

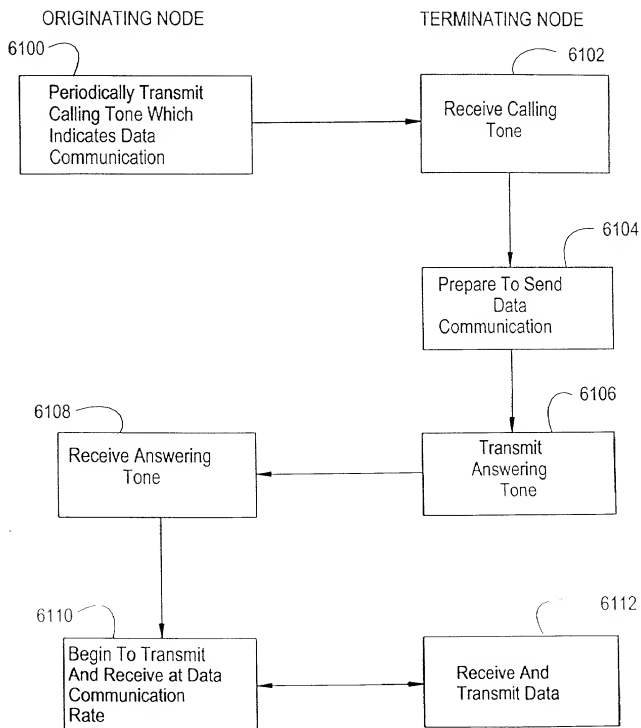


FIG. 70

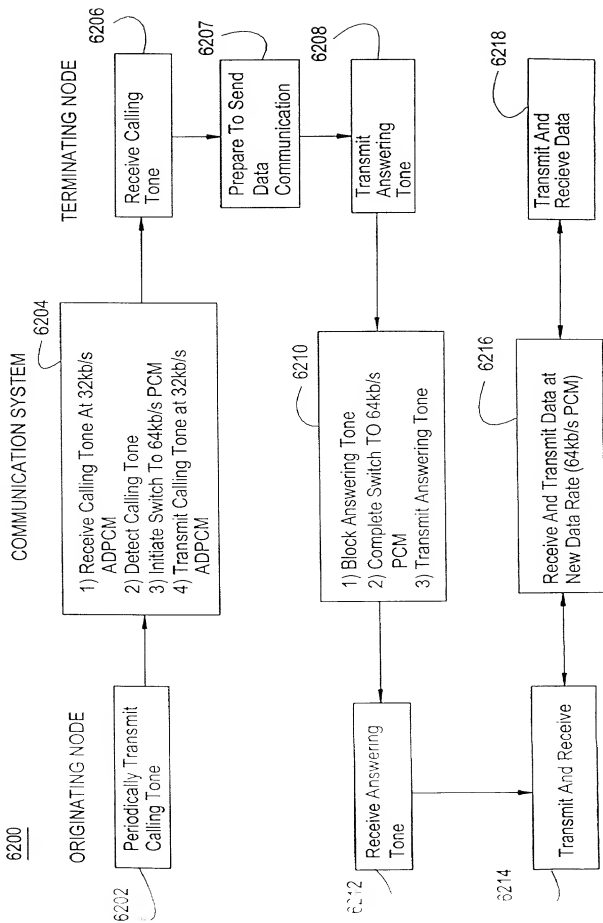


FIG. 71

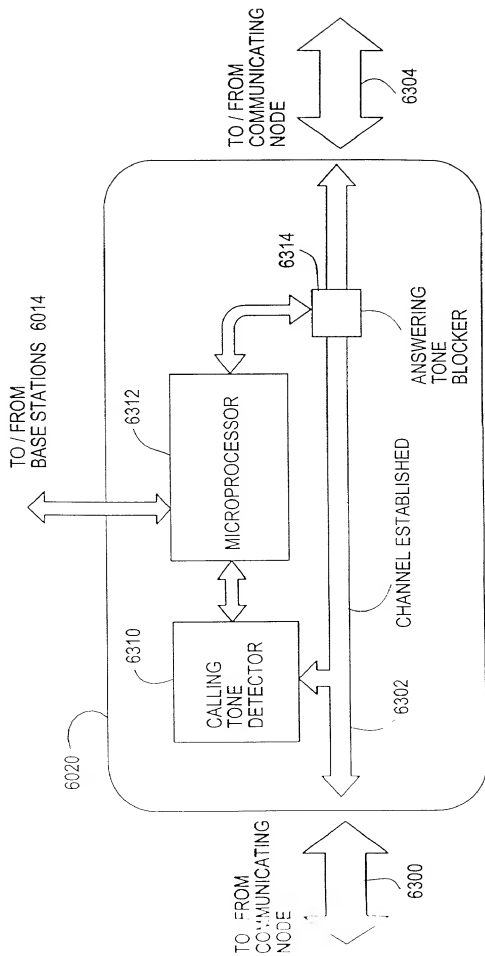
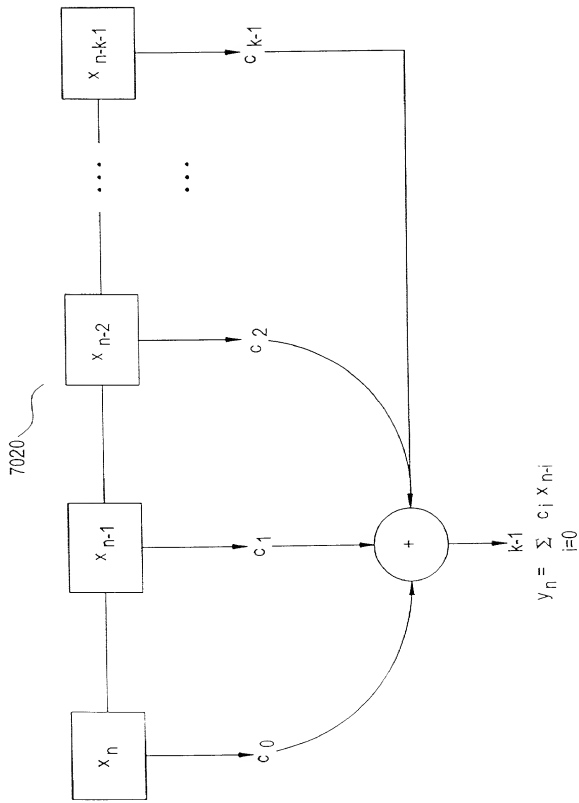


FIG. 72  
PRIOR ART



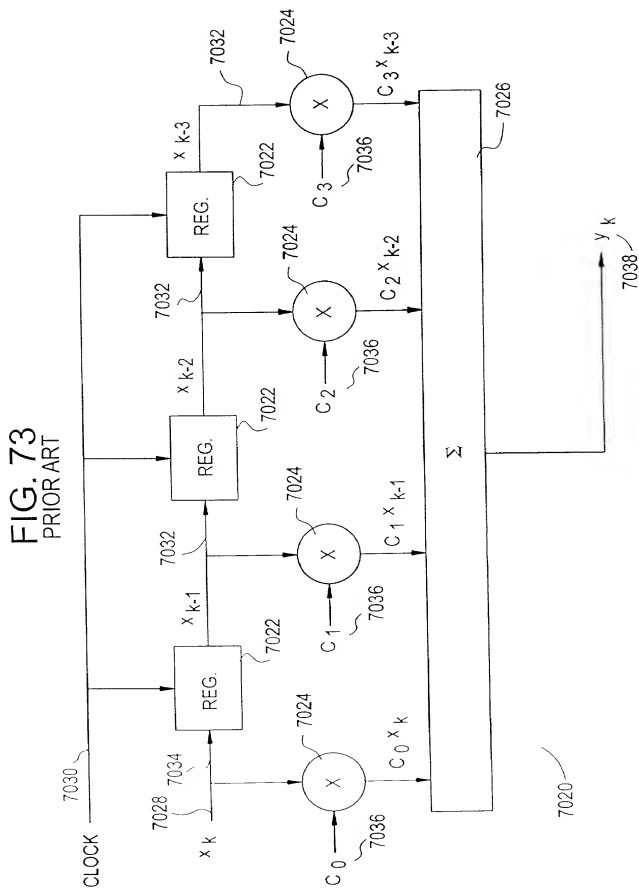




FIG. 74  
PRIOR ART

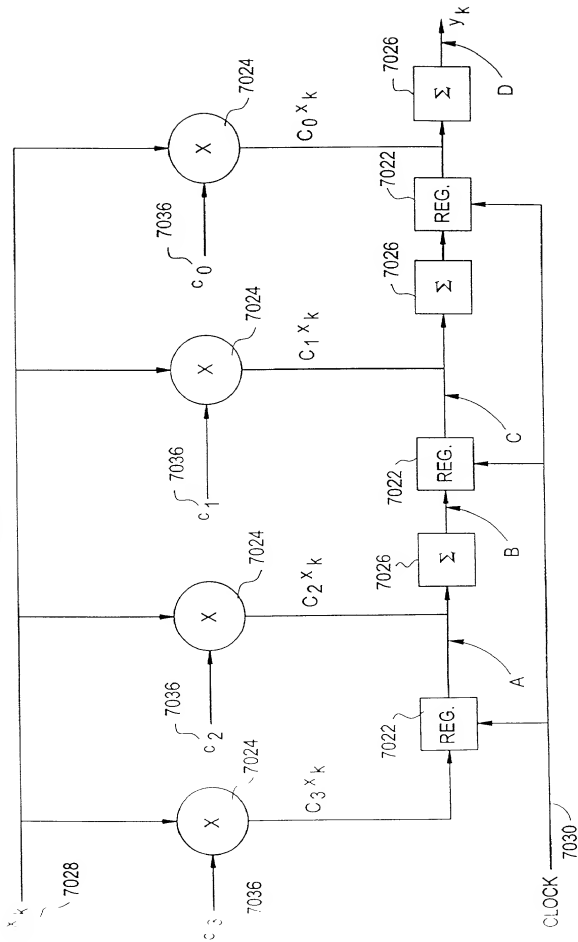
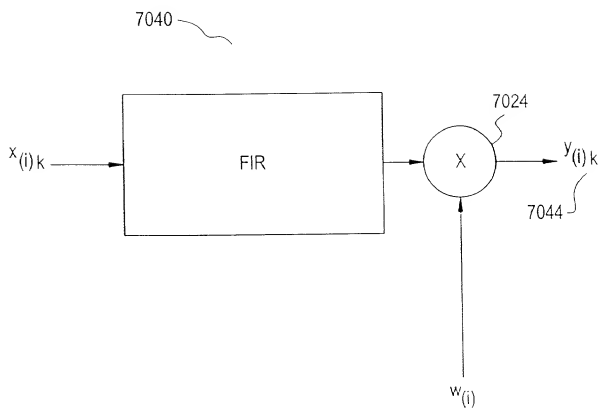
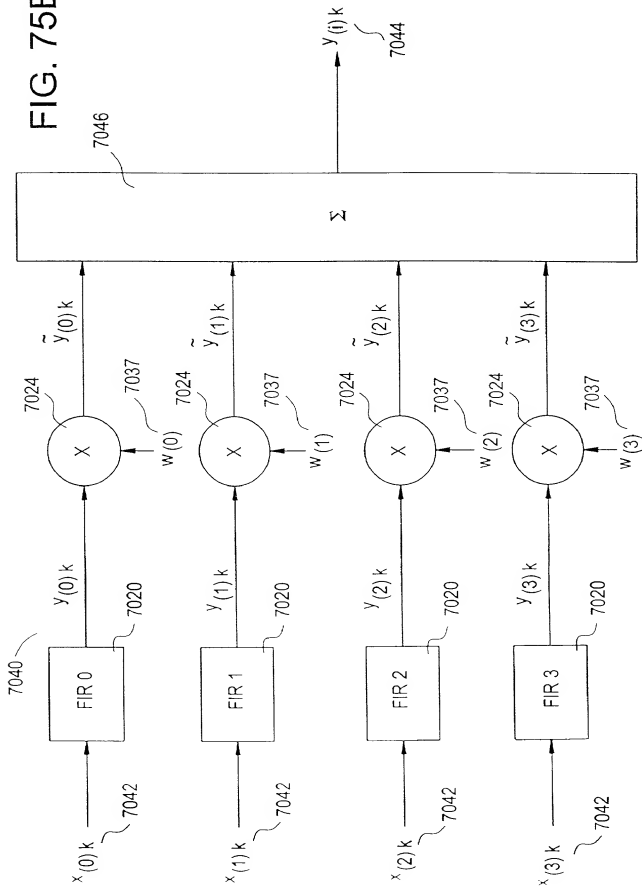


FIG. 75A





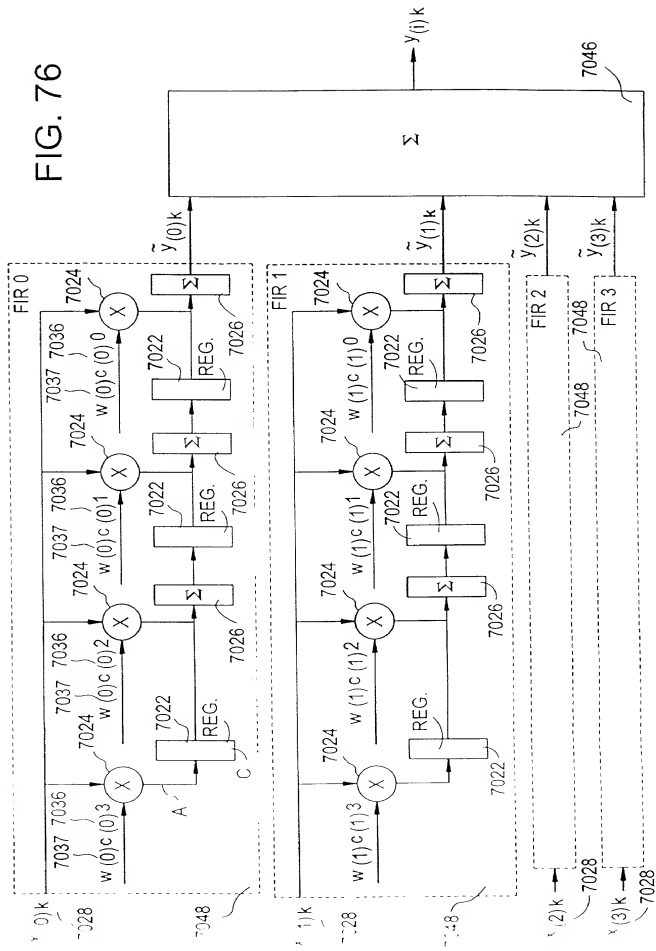


FIG. 77

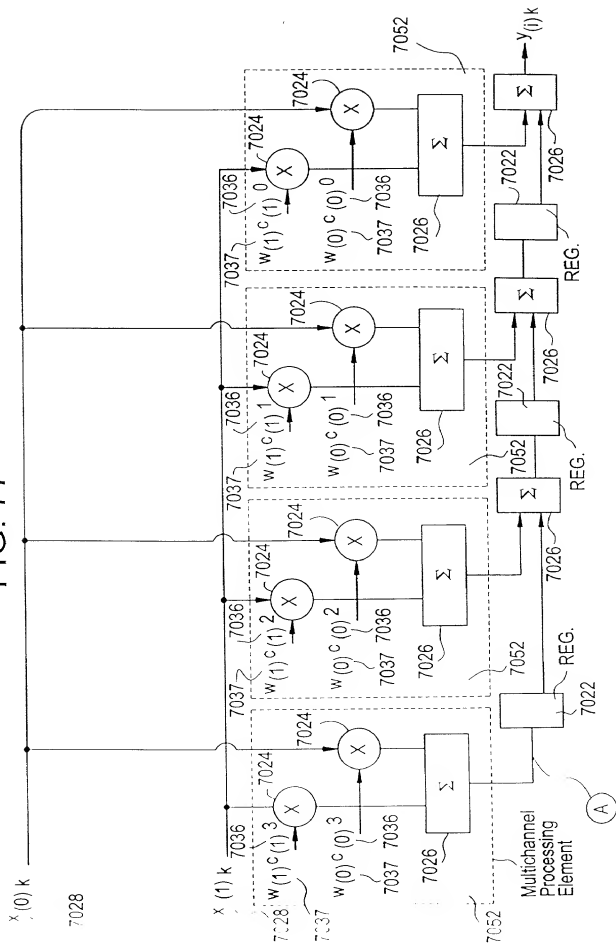


FIG. 78

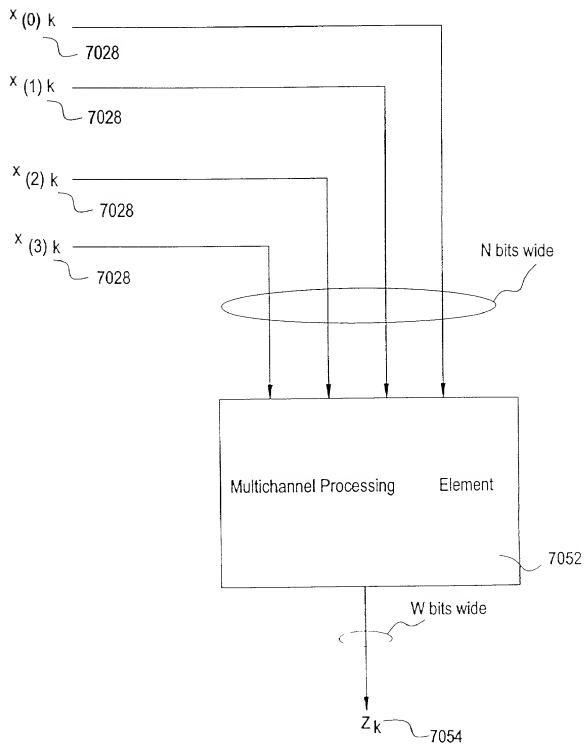


FIG. 79A

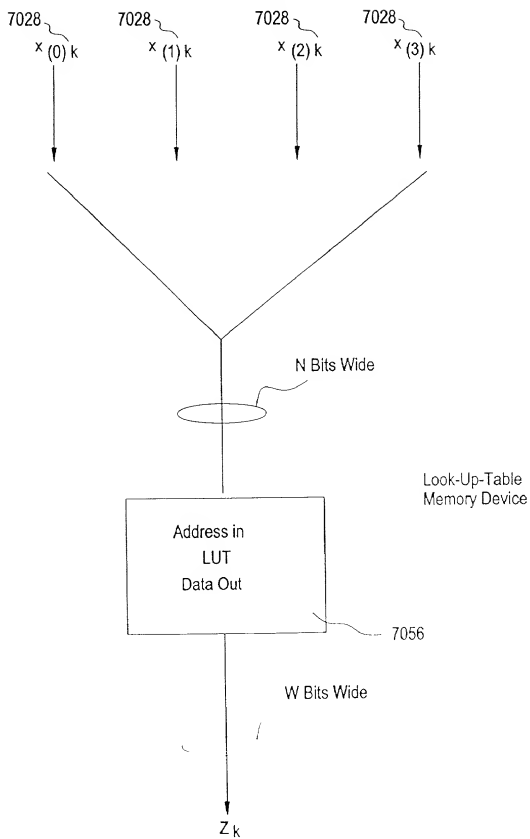


FIG. 79B

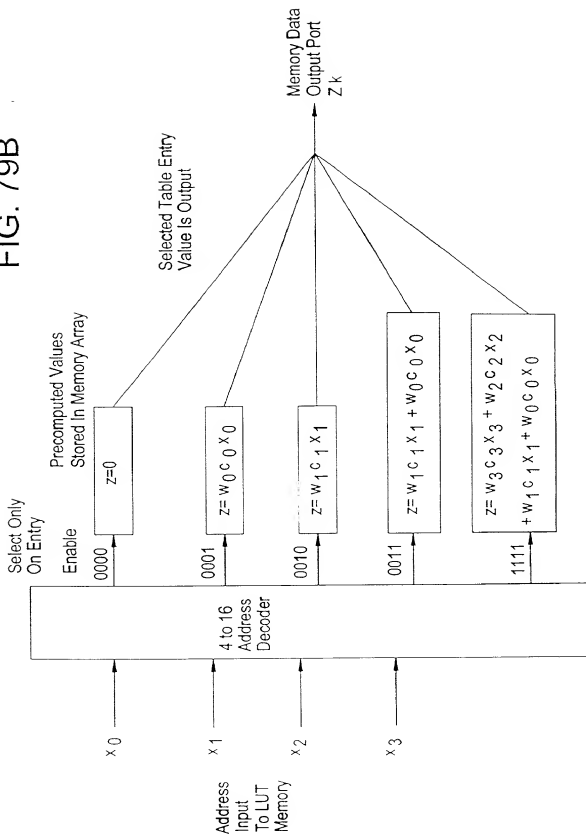




FIG. 80

